pdp11

DL11
asynchronous
line interface
engineering drawings

digital

DL11
asynchronous
line interface
engineering drawings

digital equipment corporation · maynard, massachusetts

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET ☐☐☐☐

PRINT SET #1

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-YA-1
CABLE ASSEMBLY (KL8/E)		D-IA-7008360-Ø-Ø
SOFTWARE LIST		A-SL-DL11-Ø-4
ACCESSORY LIST		A-AL-DL11-Ø-5
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

PRINT SET #2

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C		D-UA-BCØ5C-Ø-Ø
FILTER NETWORK		B-CS-G8ØØØ-Ø-1
MODEM TEST CONN		D-CS-H315-Ø-1
SOFTWARE LIST		A-SL-DL11-Ø-4
ACCESSORY LIST		A-AL-DL11-Ø-5
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

PRINT SET #3

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C		D-UA-BCØ5C-Ø-Ø
CABLE ASSEMBLY (KL81E)		D-IA-7008360-Ø-Ø
MODEM TEST CONN.		D-CS-H315-Ø-1
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

UNIT VARIATIONS

VAR	TITLE	PRINT SET DL11-1	PRINT SET DL11-2
DL11-A	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-B	ASYNC LINE INTERFACE, EIA	0	1
DL11-C	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-D	ASYNC LINE INTERFACE, EIA	0	1
DL11 E	ASYNC LINE INTERFACE, DATA SET	0	1

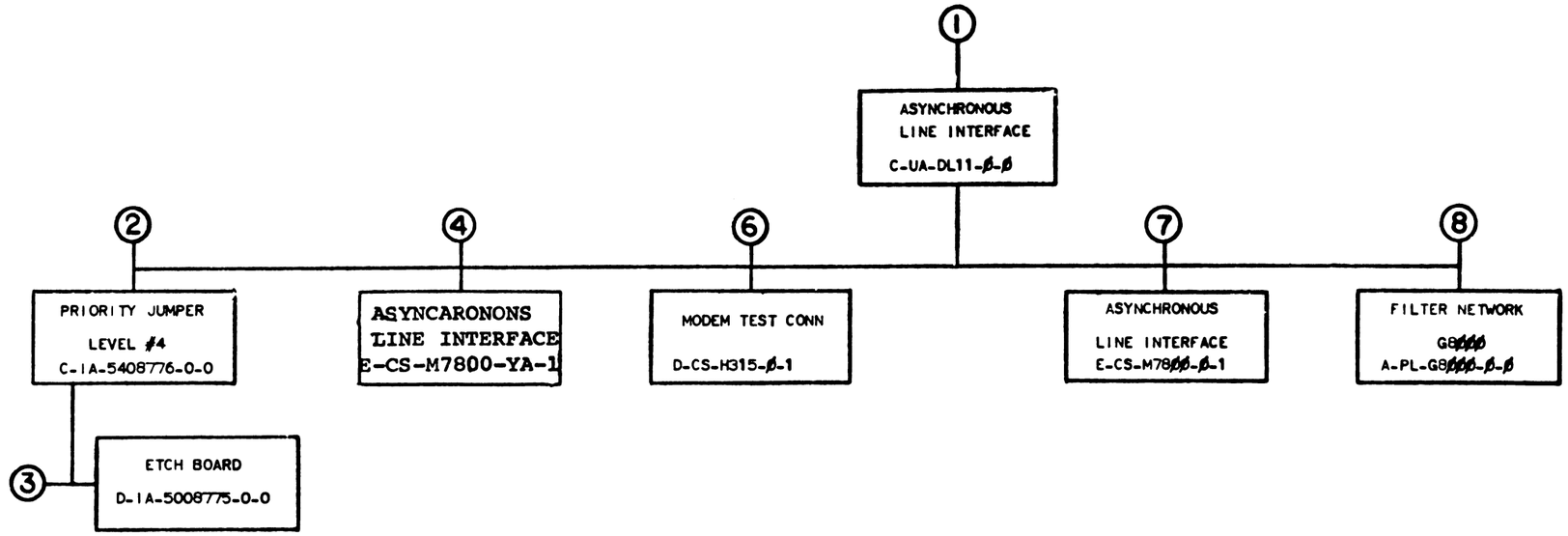
REVISIONS	DATE	CHG. NO.	REV
	2-76	REDRAWN DL11-00009	K

USED ON OPTION/MODEL			
SHEET 1 OF 3			

DRN. M. Pierce	DATE 4-28-72	TITLE ASYNCHRONOUS LINE INTERFACE	
CHK'D. R. Cook	DATE 5-9-72		
PROJ ENG. P.E.Janson	DATE 5-11-72		
PROD. J.McIntyre	DATE 5-15-72	SIZE B / CODE DD / NUMBER DL11-Ø	REV K
FIELD SERV. R. Evans	DATE 5-15-72	DIST	

EN-01062-1A-1-R572-(325)

DEB 106



TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	SHEET 2 OF 3	B	DD	DL11 - Ø	K

ELECTRICAL

CUSTOMER PRINT SET DLI1-1	DLI1-2	DLI1-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X	X	X		1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
X	X	X			A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
	X	X			D-UA-BCØ5C-Ø-Ø	#	1	CABEE, MODEM, BCØ5C	
X		X			D-IA-7008360-0-0	#	1	CABLE, ASSEMBLY (KL8/E)	
					A-SP-DL11-1-1	*	11	ENGINEERING SPECIFICATION	
X	X	X			A-SP-DL11-Ø-2	F	9	INSTALLATION PROCEDURE	
					A-SP-DL11-Ø-3	B	8	TEST PRODEDURE (TEST & ACCEPTANCE)	
X	X				A-SL-DL11-Ø-4	*	1	SOFTWARE LIST	
X	X				A-AL-DL11-Ø-5	C	1	ACCESSORY LIST	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					B-CS-5408776-0-1		1	CIRCUIT SCHEMATIC	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	MODULE ECO HISTORY	
				3.	C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
X				4	E-CS-M7800-YA-1	#	6	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-YA-4		1	X-Y COORDINATE HOLE LOCATION	
					D-AH-M7800-YA-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-M7800-YA-6		1	MODULE ECO HISTORY	
	X	X		6.	D-CS-H315-Ø-1	#	1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-H315-Ø-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
X	X	X		7.	E-CS-M7800-Ø-1	#	7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M7800-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M7800-Ø-6		1	MODULE ECO HISTORY	
	X			8.	A-PL-G8000-Ø-Ø		1	FILTER NETWORK	
					B-CS-G8000-Ø-1	#	1	CIRCUIT SCHEMATIC	
					K-CO-G8000-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8000-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8000-Ø-6		1	MODULE ECO HISTORY	

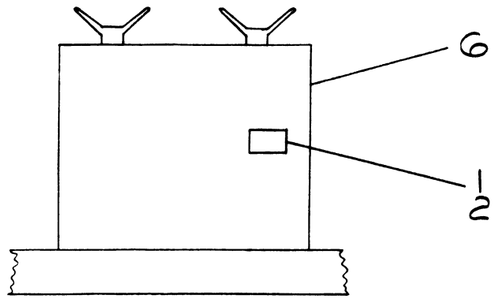
MECHANICAL

CUSTOMER PRINT SET DLI1-1	DLI1-2	DLI1-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
				1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
					A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
					D-UA-BCØ5C-Ø-Ø		1	CABLE, MODEM BCØ5C	
					D-IA-7008360-0-0		1	CABLE ASSEMBLY (KL8/E)	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	ASSY/DRILLING HOLE LAYOUT	
				3.	D-IA-5008775-0-0		1	ETCH BOARD	
					C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
				6.	D-CS-H315-Ø-1		1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
				7.	E-CS-M7800-Ø-1		7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M7800-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M7800-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8000-Ø-Ø		1	FILTER NETWORK	
					K-CO-G8000-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8000-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8000-Ø-6		1	MODULE ECO HISTORY	

TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	3 OF 3	B	DD	DLII-Ø	K

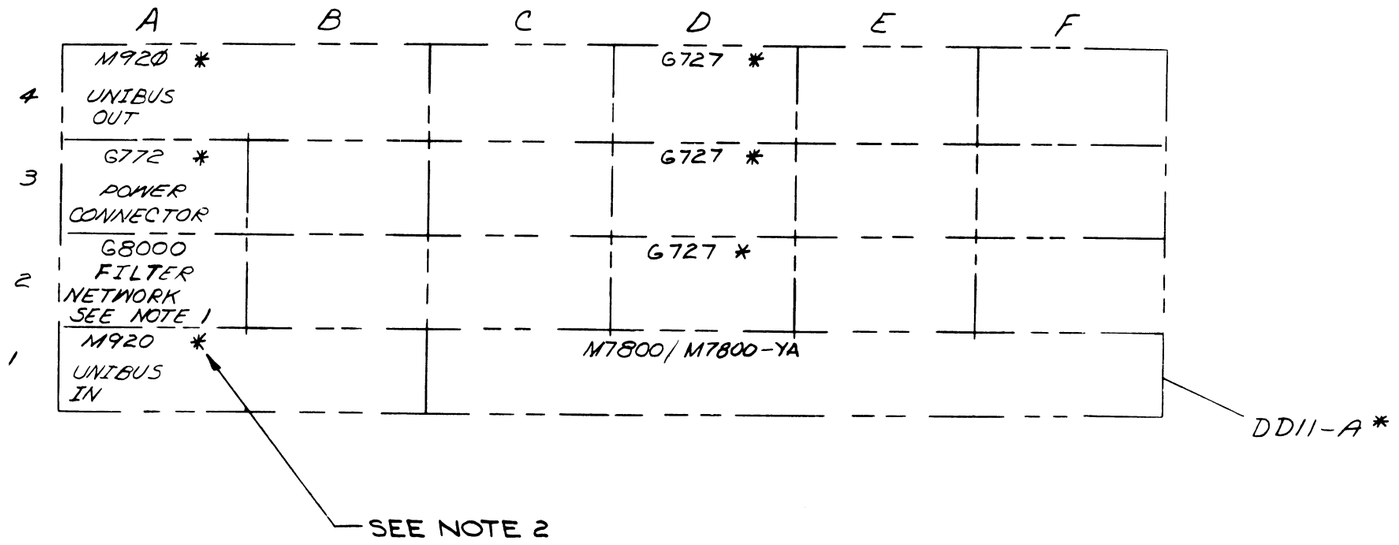
DRB 108

DEC 16-(325)-1062-2-N871



NOTES:

1. G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALLATION REQUIRES 2 WIRES TO BE ADDED.
   A03V2 - A02V2
   A02N2 - CXXU1
   WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL 11.
2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.



REVISIONS	CHANGE NO.	REV.	BY
CHK.	DL11-00001	A	R JANSON 7-17-72
	DL11-00002	B	JANSON 12-5-72
	DL11-00005	C	L. CONDON 7-31-73
	DL11-00006	D	CONDON 9-21-73
	DL11-00008	E	L. CONDON 4-4-75
	DL11-00009	F	J. MCINTYRE 12-FEB-76

DEC FORM NO. DRC 100-A

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN. M Price	DATE 7/18/72	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. J Fenerson	DATE 9-29-72	
ENG. D E Johnson	DATE 5-11-72	
PROJ ENG. D E Johnson	DATE 5-11-72	TITLE ASYNCHRONOUS LINE INTERFACE
PROD. J McIntyre	DATE 5-15-72	

NEXT HIGHER ASSY. B-DD-DL11-0

SCALE NONE

SHEET 1 OF 1

SIZE	CODE	NUMBER	REV.
C	UA	DLH-[redacted]	F

DIST. G

SIZE CODE CUA NUMBER DL11-0-0 REV. F

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY M. PIERCE DATE 4/27/72	CHECKED J. FERGUSON DATE 4/27/72	SECTION 1
ENG P. E. JANSON DATE 5/11/72	PROD J. McGuire DATE 5/15/72	ISSUED SECT. 1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1
3	D-UA-BCØ5C-25	CABLE MODEM BCØ5C	-	1	-	1	1
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-
5	D-CS-H315-Ø-1	MODEM TEST CONNECTOR	-	-	-	-	A/R See Note 2
6	E-CS-M7800-Ø-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1
7	~~A-PL-8000Ø-Ø-Ø~~	~~FILTER NETWORK~~	~~=~~	~~A/R~~	~~A/R~~	~~A/R~~	~~A/R See Note 2~~
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R See Note 3
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-
10	9008269	TRANSPARENT VINYL TAPE	A/R				
	NOTES:						
	1. G8000 IS REQUIRED ONLY IN PDP11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A						
	2. ONE H315 PER PDP11 SYSTEM						
	3. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE OR BY THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.						
	4. APPLY TAPE TO TOP SURFACES OF CRYSTAL AND MOUNTING BRACKETS TO INSULATE FROM ADJACENT MODULES.						
	5. PRIORIY LEVELS 5.6, or 7 MAY BE SPECIFIED BY THE CUSTOMER OR THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.						

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø	A	PL	DL11-Ø-Ø	F	DL11-00009
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870

NOTES:

1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

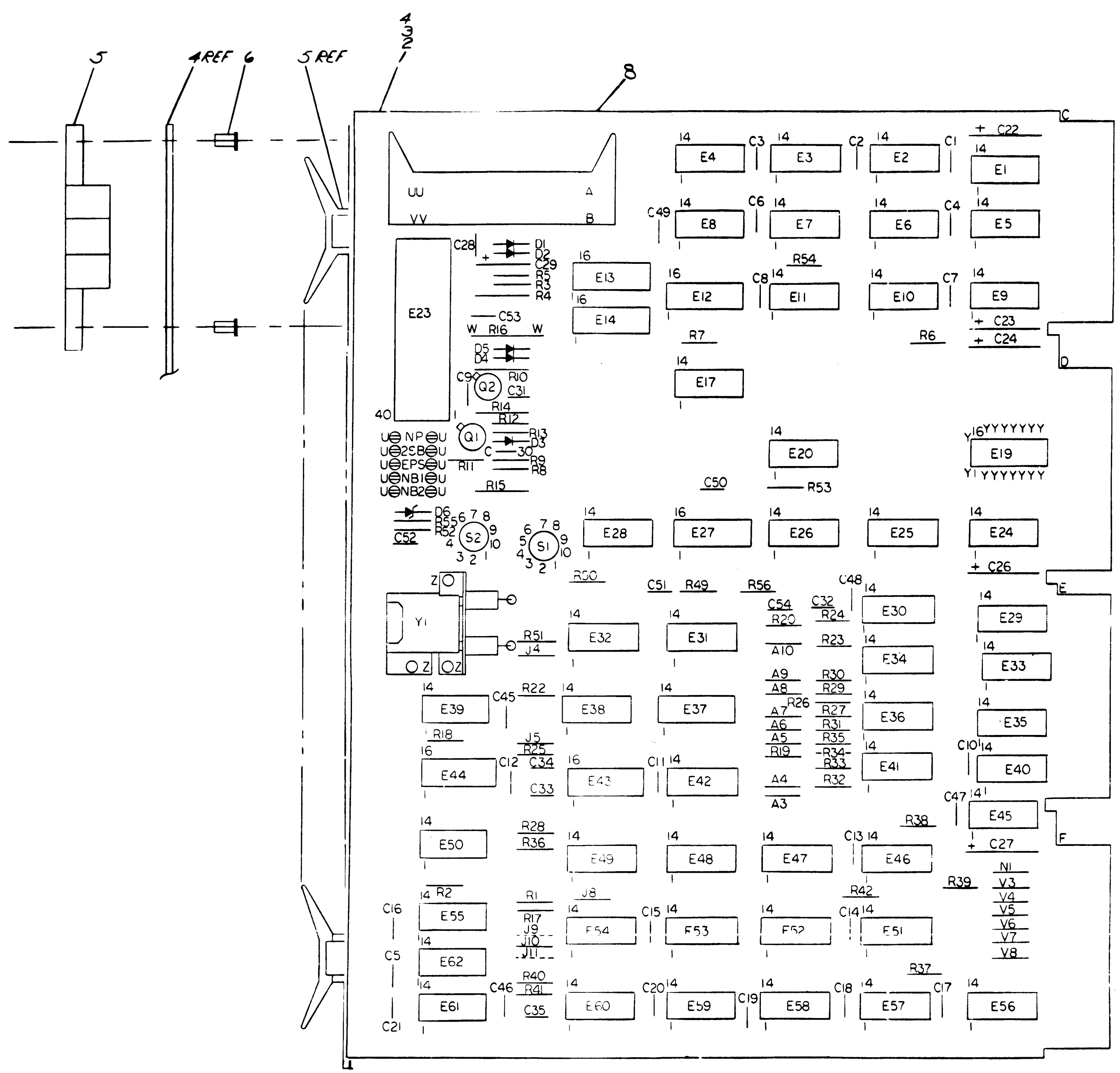
2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J6, J8-J10, V3-V8, AND N1.

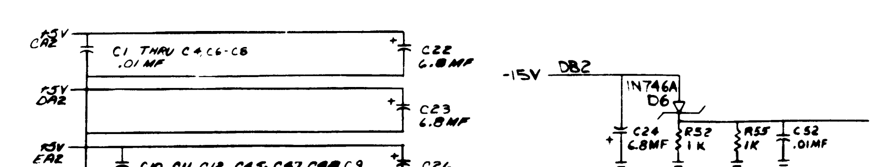
3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (Z).

4.) DEC 8640S WERE PHASED IN AS 380 REPLACEMENTS ANY 380 FAILURES SHOULD BE REPLACED BY 8640 S, EXCEPT E28. E28 MUST BE REPLACED WITH A 7380 CHIP.

PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F





DEC 74161	8	16	—	—
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—
IC TYPE	GND	+5V	+V	-12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E28	IC DEC 7380	1910390	69
A/R		INSULATION TUBING	91 7256-11	68
1	R3	RES 750Ω 1/4W 5%	1301401	67
1	R38	RES 390Ω 1/4W, 5%	1300309	66
1	D6	DIODE 1N746A	1104860	65
2	Q1, Q2	TRANSISTOR 6534D	1503409-00	64
1	C53	CAP 100PF 100V 5% DIPPED MICA	1000016	63
1	C54	CAP 560PF 100V 5% DIPPED MICA	1000025	62
2	C50, C51	CAP .047MF CERAMIC	1009678	61
1	E27	IC DEC 74161	1910650	60
2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
1	C32	CAP 470PF 100V 5% DIPPED MICA	1000024	58
1	C31	CAP 1000PF 100V 5% DIPPED MICA	1000042	57
29	C1-C21, C28, C30, C45-C49, C52	CAP .01UF 100V 20% CERAMIC DISC	1001610	56
1	C29	CAP .47UF 35V 10% TANT	1005965	55
5	C22-C24, C26, C27	CAP 6.8UF 35V 20% TANT	1000067	54
1	C33	CAP 150PF 100V 5% DIPPED MICA	1000019	53
2	R14, R15	RES 1.5K 1/2W 5%	1300394	52
5	R23, R26, R40, R52, R55	RES 1K 1/4W 5%	1300365	51
1	R41	RES 47Ω 1/4W 5%	1300202	50
1	R10	RES 68Ω 1/2W 10%	1300220	49
1	R5	RES 82Ω 1/4W 5%	1301477	48
1	R24	RES 100Ω 1/4W 5%	1300229	47
1	R11	RES 130Ω 1/4W 5%	1300230	46
[illegible]	R42, R57	RES 180Ω 1/4W 5%	1301322	45
1	R53	RES 220Ω 1/4W 5%	1300271	44
5	D1-D5	DIODE D664 20V 100mA	1100114	43
3	R9, R13, R51	RES 470Ω 1/4W 5%	1300316	42
1	R4	RES 560Ω 1/2W 5%	1300338	41
3		NUT HEX #2-56	9006555	40
1	R16	RES 750Ω 1W 5%	1302385	39
26	R1, R2, R6, R7, [illegible] R25, R27-R37, R39, R47, R50, [illegible] R54, R56	RES 10K 1/4W 5%	1300479	38
2	R8, R12	RES 1.5K 1/4W 5%	1300391	37
1	E23	IC DEC UART	1910459	36
4	E32, E55, E61, E62	IC DEC 7474	1905547	35
2	E36, E41	IC DEC 8242	1909712	34
3	E31, E49, E59	IC DEC 7408	1910155	33
3		SCR PHIL HD PAN #2-56 X .25 LG	9006001-1	32
2	E20, E26	IC DEC 7490	1909037	31
11	E1, E2, E5, [illegible]-E9, E11, E30, E47, E51, E56	IC DEC 8881	1909705	30
2		AUGAT 8000 FG-1	1202812	29
1	E43	IC DEC 74123	1910436	28
3	E48, E57, E52	IC DEC 74H74	1909667	27
3	E42, E54, E58	IC DEC 7400	1903575	26
1	E10	IC DEC 7413	1909989	25
2	E50, E53	IC DEC 7402	1909004	24
7	E3, E4, E33, E35, E40, E45, E46	IC DEC [illegible]	[illegible]1469	23
1	E12	IC DEC 74153	1909937	22
1	E60	IC DEC 74H04	1909931	21
1	E25	IC DEC 7492	1909053	20
4	E6, E17, E38, E39	IC DEC 7404	1909686	19
1	E24	IC DEC 7493	1909054	18
1	E34	IC DEC 7410	1903576	17
1	E29	IC DEC 314	1909704	16
1	E37	IC DEC 7442	1910046	15
1	E44	IC DEC 8271	1909615	14
2	E13, E14	IC DEC 74175	1910651	13
1		BRACKET, CRYSTAL HOLDER	5302825	12
1		BRACKET, CRYSTAL HOLDER	5303154	11
1	E19	IC SOCKET	1209838	10
2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1210012-1	9
1		40 PIN CONNECTOR BERG	1209941	8
10		SPLIT LUGS	9006735	7
8		EYELET #GS4-7 E.B. STIMPSON	9006732	6
4		HANDLE, FLIP-CHIP, MAGENTA	9008337-06	5
1		ETCHED CIRCUIT BOARD	5008[illegible]	4
REF		MODULE ECO HISTORY	[illegible]	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7800-[illegible]	2
REF		X-Y COORDINATE HOLE	K-CO-[illegible]	1

PARTS LIST

ETCH BOARD REV H

DEC NO.	EIA NO.
6534D	MPS6534
1N746A	1N4M3.3AZ
D664	1N3606

SEMICONDUCTOR CONVERSION CHART

NEXT HIGHER ASSY

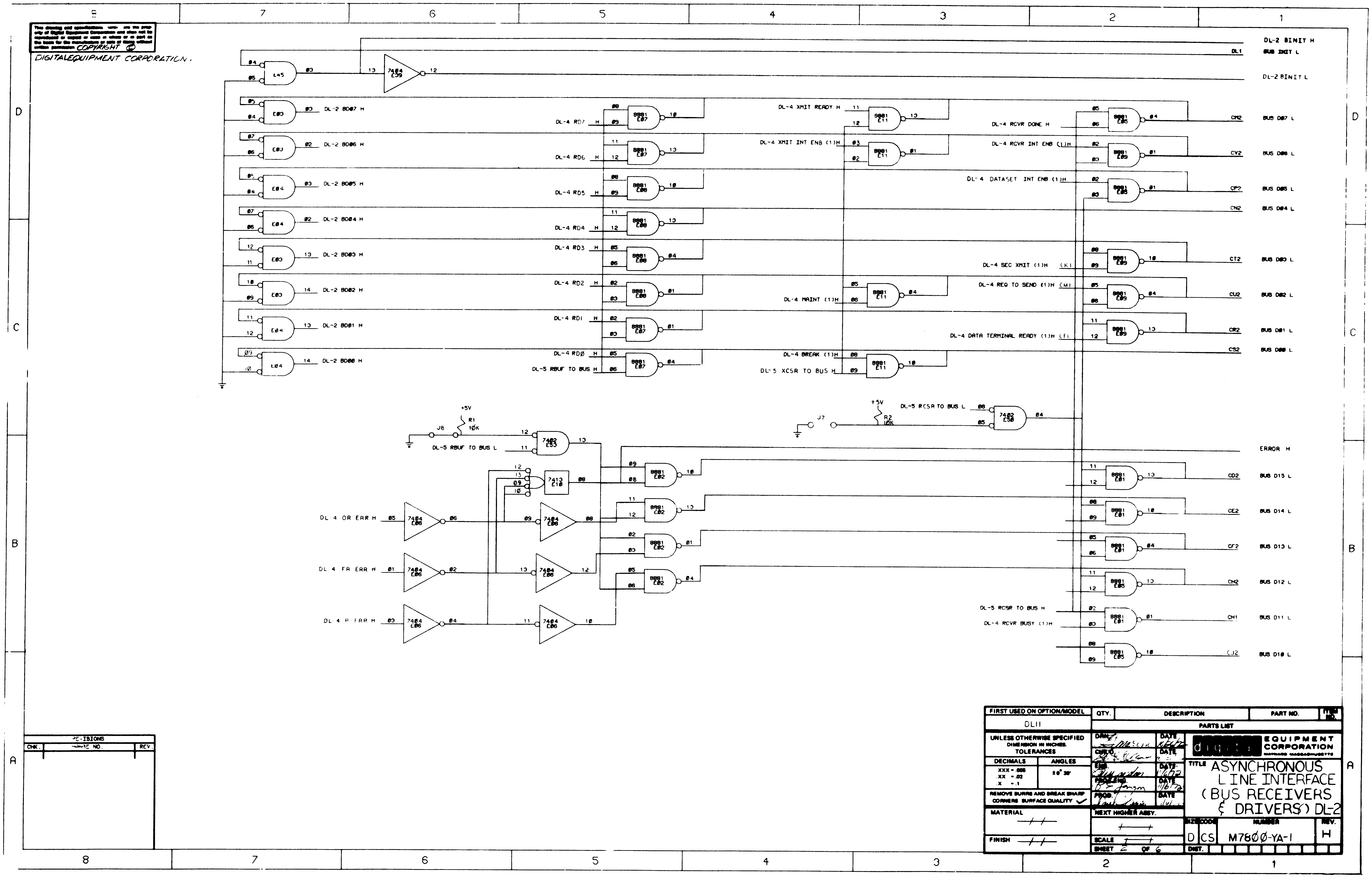
SCALE —

SHEET 1 OF 6

[redacted] EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

E CS M7800-YA-1 H



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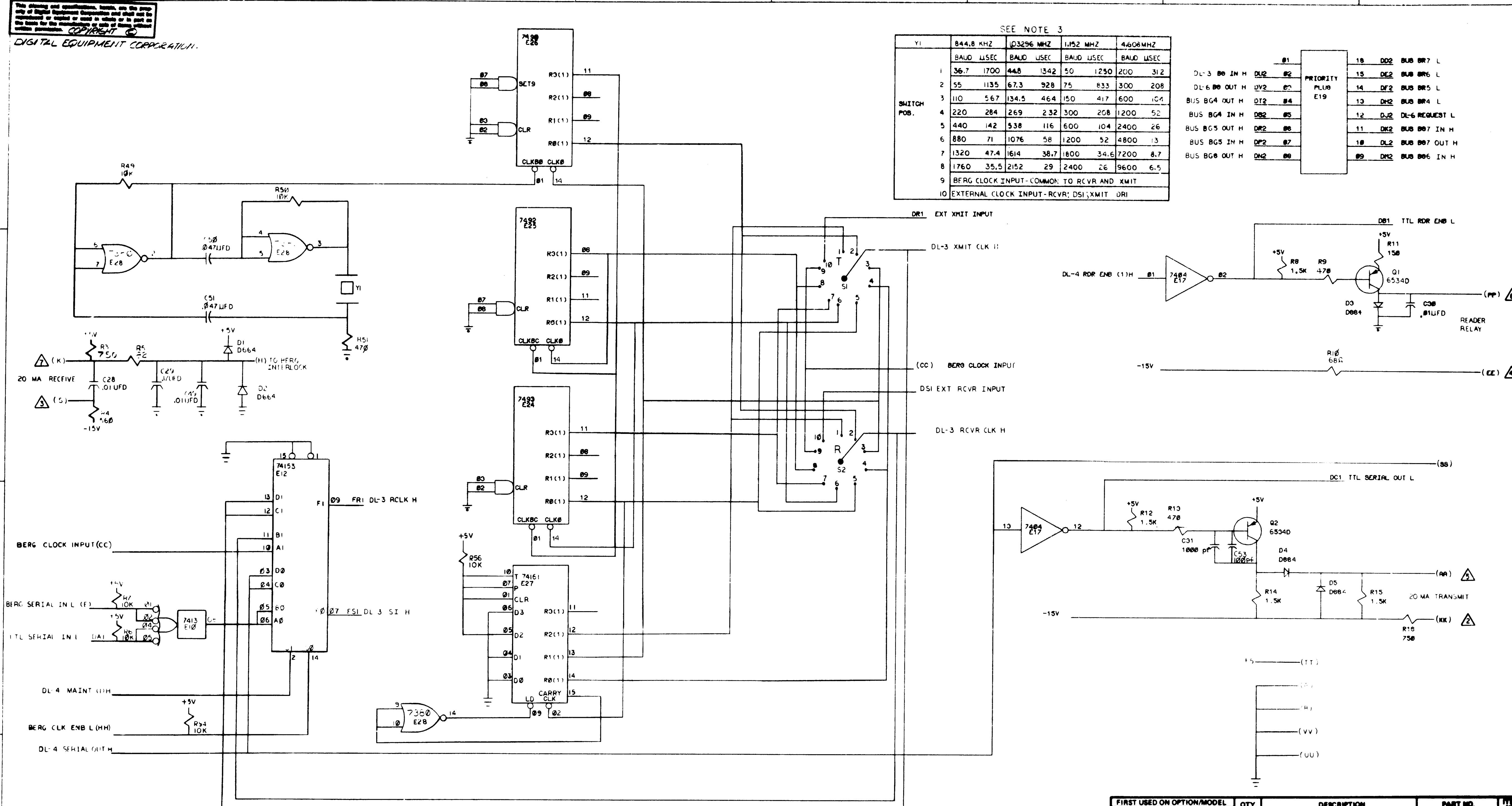
DIGITAL EQUIPMENT CORPORATION.
DL-2 BINIT H
DL1 BUS INIT L
DL-2 BINIT L
DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1
DL-4 RDØ H
DL-5 RBUF TO BUS H
DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H
DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 REQ TO SEND (1)H
DL-4 DATA TERMINAL READY (1)H
CM2 BUS D07 L
CV2 BUS D06 L
CP2 BUS D05 L
CN2 BUS D04 L
CT2 BUS D03 L
CU2 BUS D02 L
CR2 BUS D01 L
CS2 BUS D00 L
+5V
R1 10K
J8
DL-5 RBUF TO BUS L
J7
R2 10K
DL-5 RCSR TO BUS L
ERROR H
DL 4 OR ERR H
DL 4 FR ERR H
DL 4 P ERR H
DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H
CD2 BUS D15 L
CE2 BUS D14 L
CF2 BUS D13 L
CH2 BUS D12 L
CH1 BUS D11 L
CJ2 BUS D10 L
REVISIONS
CHK.
REV.
FIRST USED ON OPTION/MODEL
DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS
ANGLES
XXX = .005
XX = .02
X = .1
±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DRN.
CHK'D.
ENG.
PROD.
DATE
NEXT HIGHER ASSY.
SCALE
SHEET 2 OF 6
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2
SIZE D
CODE CS
NUMBER M7800-YA-1
REV. H
DIST.



SEE NOTE 3

Y1		844.8 KHZ		1.03296 MHZ		1.152 MHZ		4.608 MHZ	
		BAUD	μSEC	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC
SWITCH POS.	1	36.7	1700	44.8	1342	50	1250	200	312
	2	55	1135	67.3	928	75	833	300	208
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	208	1200	52
	5	440	142	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	13
	7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
	8	1760	35.5	2152	29	2400	26	9600	6.5
	9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT - RCVR: DSI; XMIT DRI							

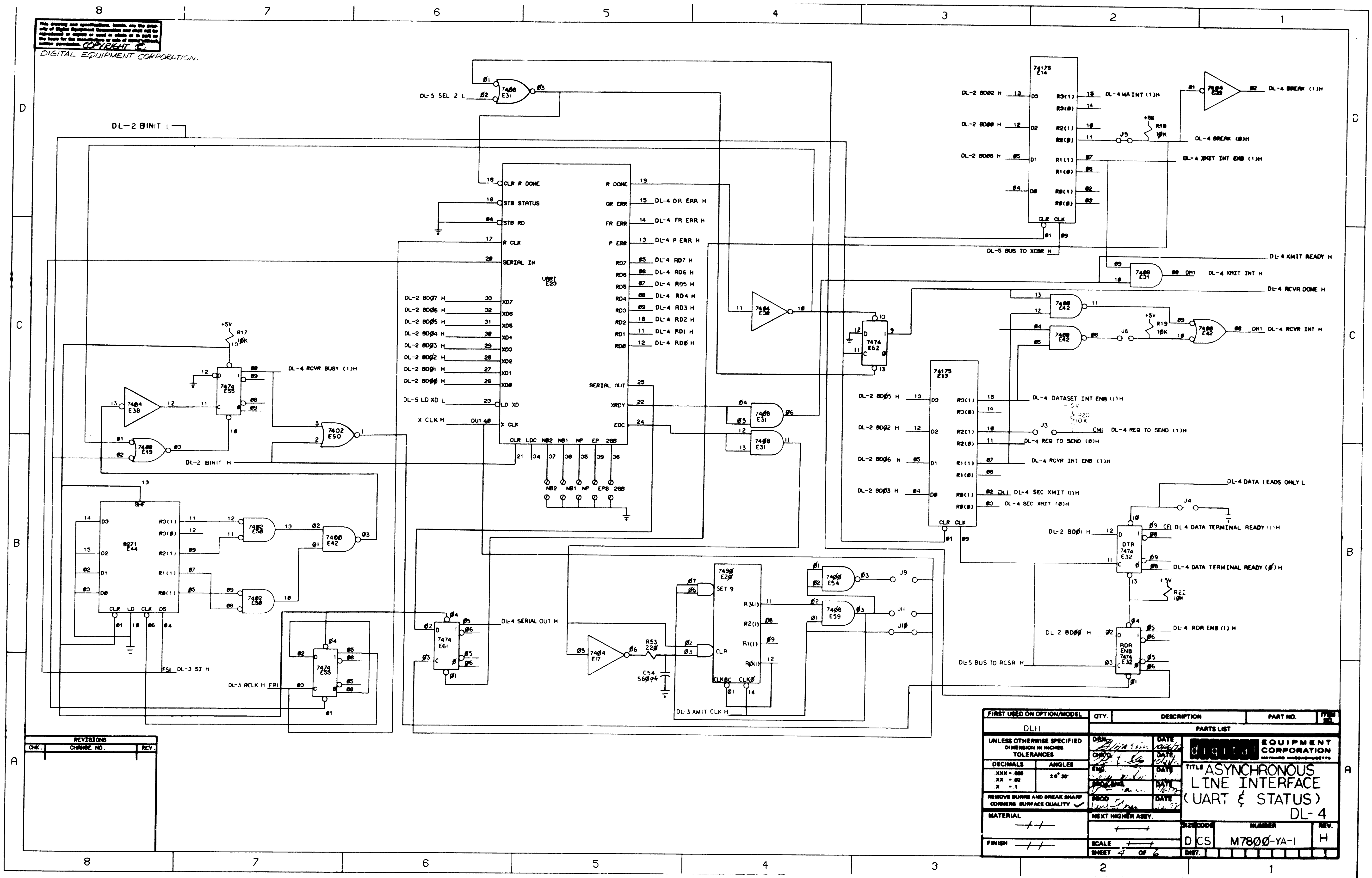
NOTES:

1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD [illegible] TAL OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION [illegible] N WHICH [illegible] THE [illegible]

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	DL11
QTY. / DESCRIPTION / PART NO. / ITEM NO.	PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	DECIMALS: .XXX = .005, .XX = .02, .X = .1; ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	✓
MATERIAL	—
FINISH	—
NEXT HIGHER ASSY.	—
SCALE	—
SHEET	3 OF 6
TITLE	ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3
SIZE	D
CODE	CS
NUMBER	M7800-YA-1
REV.	H

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS



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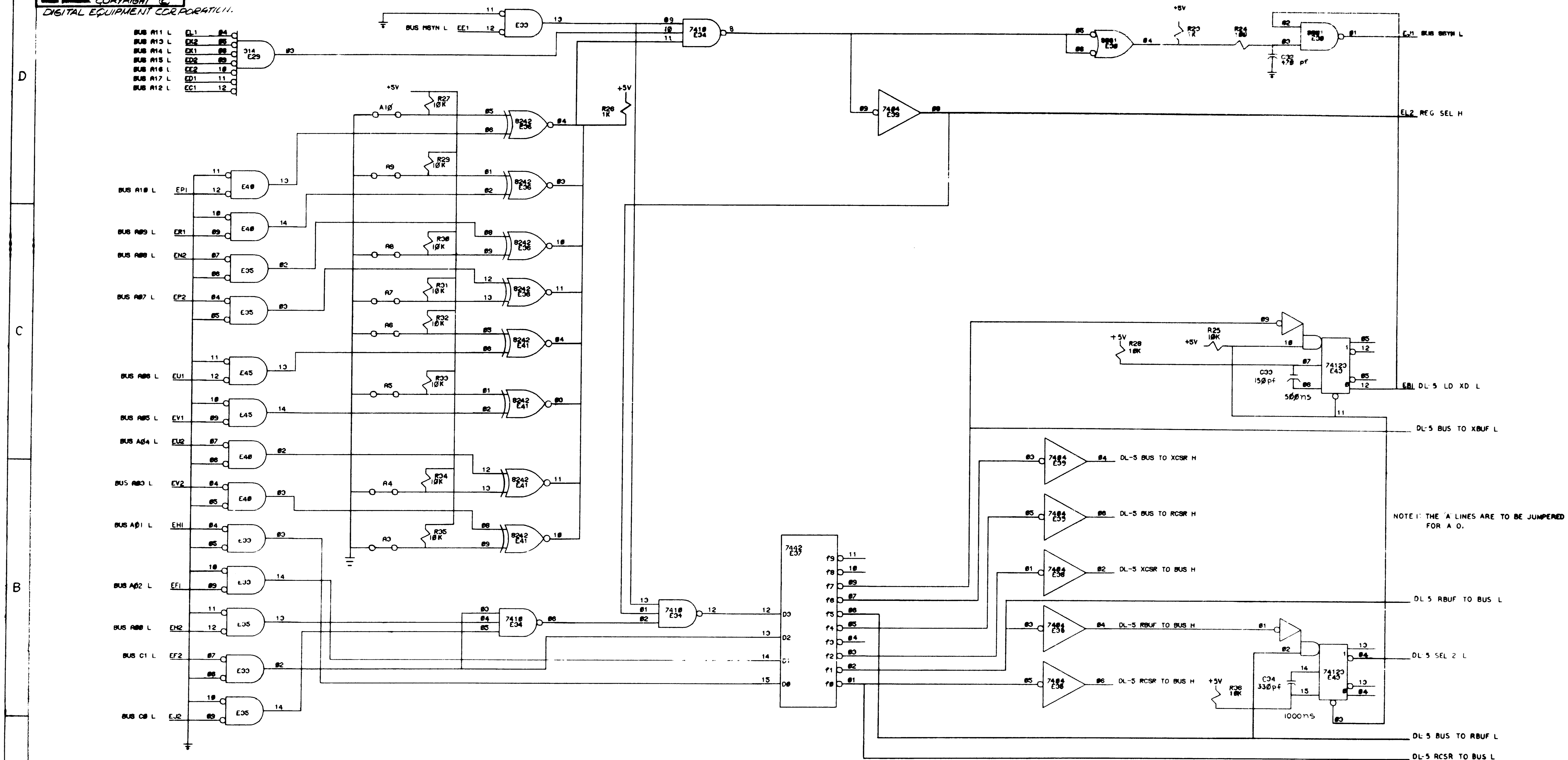
DIGITAL EQUIPMENT CORPORATION
DL-5 SEL 2 L
DL-2 BINIT L
UART E23
CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
R DONE
OR ERR
FR ERR
P ERR
SERIAL OUT
XRDY
EOC
DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RDØ H
DL-5 LD XD L
X CLK H
DL-4 RCVR BUSY (1)H
DL-2 BINIT H
FSI DL-3 SI H
DL-3 RCLK H
DL-4 SERIAL OUT H
DL 3 XMIT CLK H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-4 BREAK (Ø)H
DL-4 XMIT INT ENB (1)H
DL-5 BUS TO XCSR H
DL-4 XMIT READY H
DL-4 XMIT INT H
DL-4 RCVR DONE H
DL-4 RCVR INT H
DL-4 DATASET INT ENB (1)H
DL-4 REQ TO SEND (1)H
DL-4 REQ TO SEND (Ø)H
DL-4 RCVR INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 SEC XMIT (Ø)H
DL-4 DATA LEADS ONLY L
DL-4 DATA TERMINAL READY (1)H
DL-4 DATA TERMINAL READY (Ø)H
DL-4 RDR ENB (1) H
DL-5 BUS TO RCSR H
REVISIONS
FIRST USED ON OPTION/MODEL
DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS
ANGLES
MATERIAL
FINISH
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4
SIZE D
CODE CS
NUMBER M7800-YA-1
REV. H
SHEET 4 OF 6



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN / CHK'D / ENG / PROJ ENG / PROD — DATE

NEXT HIGHER ASSY. —

SCALE —

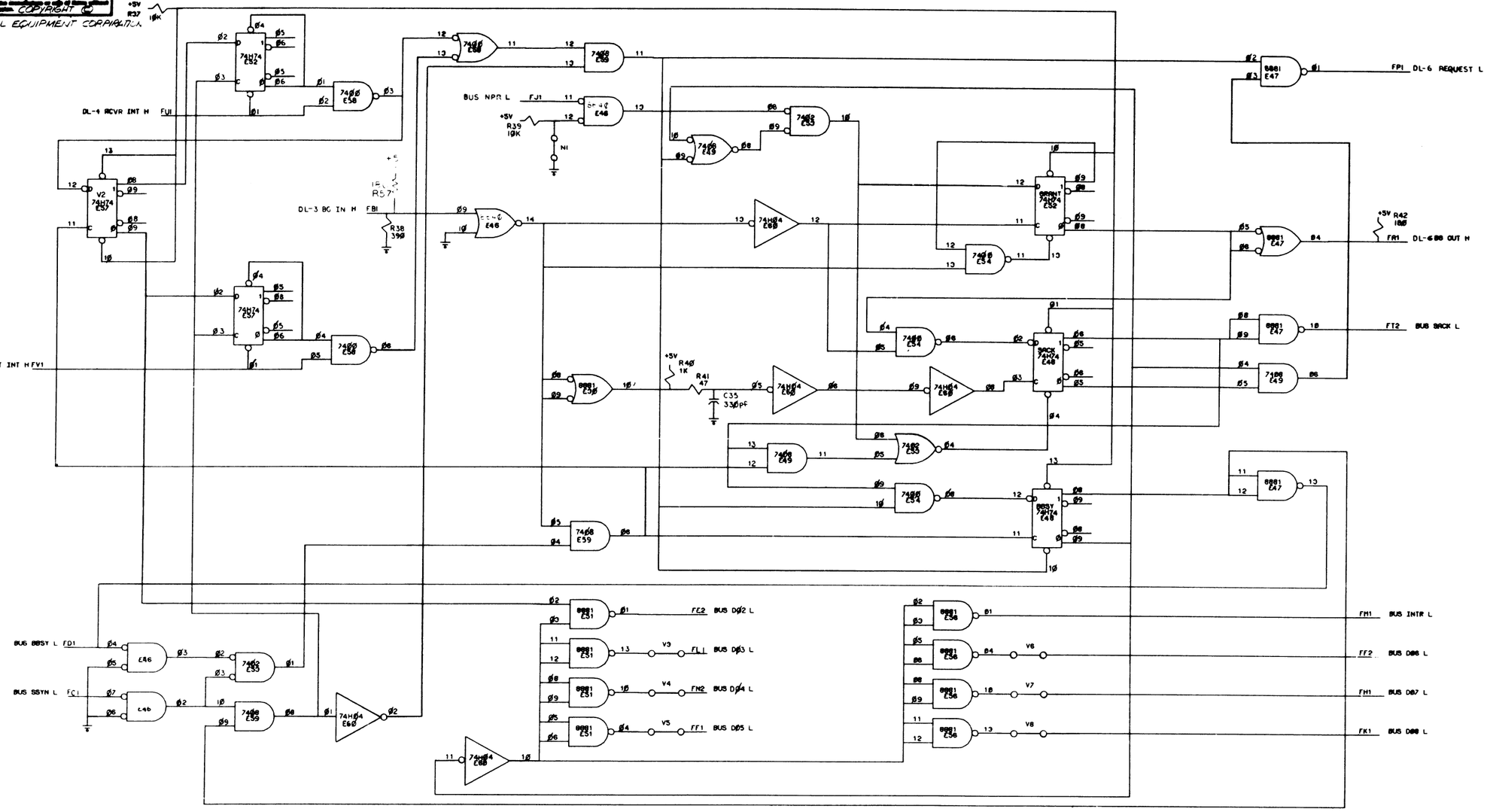
SHEET 5 OF 6

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-1	H

DIST.



NOTE: THE 'V' LINES ARE TO BE JUMPERED FOR A 1.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX ± .005, .XX ± .02, .X ± .1
ANGLES ± 0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRAW. DATE
CHK'D DATE
ENGR DATE
PROJ. MGR. DATE
PROD. DATE
NEXT HIGHER ASSY.
SCALE
SHEET 6 OF 6

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

CAGE CODE	NUMBER	REV.
D CS	M7800-YA-1	H

DIST.

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WIRE TABLE

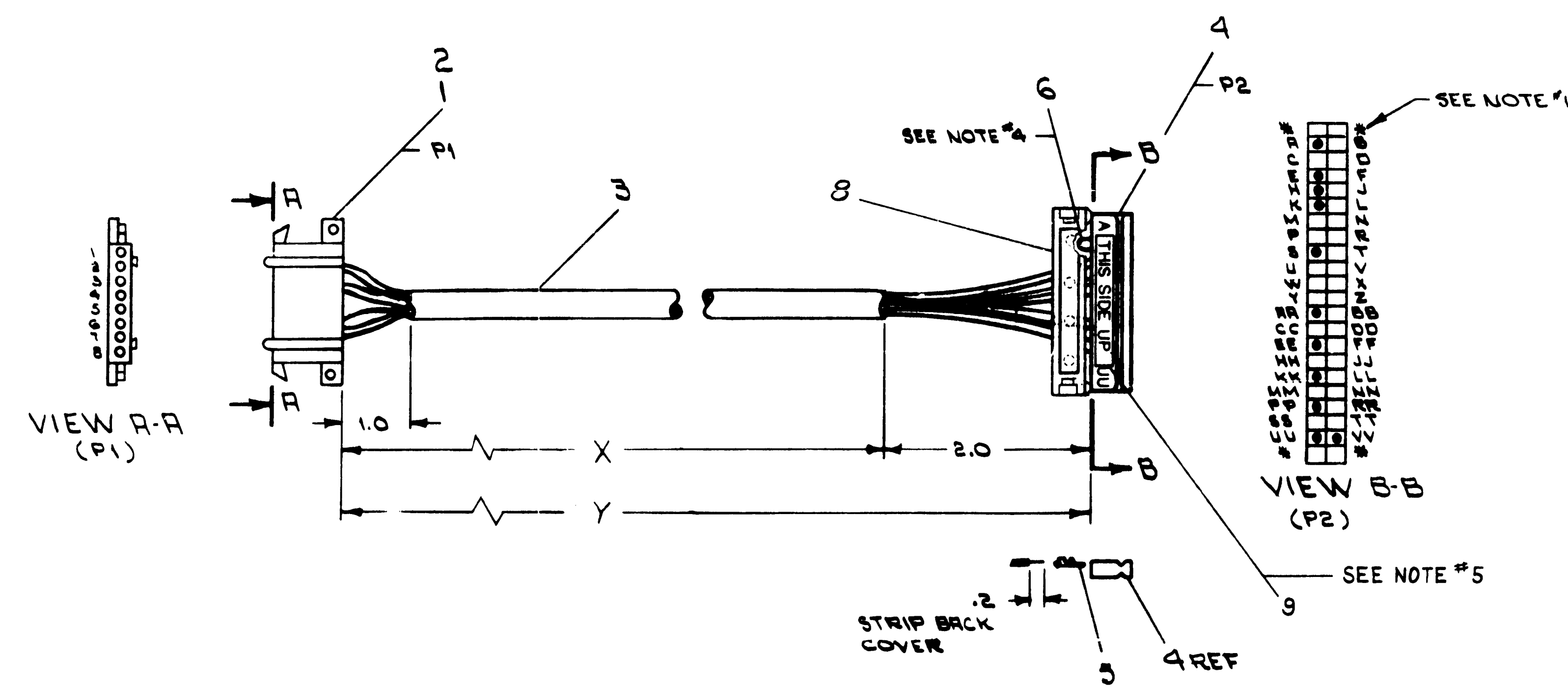
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3	↑	RED	1	P1-3	2	P2-S	↑
3,7		SHIELD	1	SEE NOTE #2	—	P2-A(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT	2	P1-5	2	P2-AA	
3,7		SHIELD	2	SEE NOTE #2	—	P2-UU(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN	3	P1-7	2	P2-K	
3,7	↓	SHIELD	3	SEE NOTE #2	—	P2-VV(NOTE #3)	↓
6	22	BLK	—	P2-E	5	P2-H	5

LEGEND

VARIATION	LENGTH X	LENGTH Y
7008360-0	25IN±1.0	27IN±1.0
7008360-1	46IN±1.0	48IN±1.0

NOTES:

1. * ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM #6 (WIRE) TO BE APPROXIMATELY ONE (1) INCH LONG.
5. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	361567	9
	STRAIN RELIEF	12 1106	8
A/R	TUB. #18 TEF. THINWALL NAT	9107278-11	7
A/R	WIRE, #22 AWG STRD TEF BLK	9107350-00	6
11	SOCKET, CRIMP # 47216	1210089-07	5
1	HOUSING, BERG # 65043-015	1210313-15	4
A/R	CABLE, BELDEN #8777-3PR SHLD	9107723-0	3
6	CONTACT MATE-N-LOCK (FEMALE)	1209379-03	2
1	CONN. MATE-N-LOCK (FEMALE)	1209340-00	1

FIRST USED ON OPTION/MODEL: PDP-8E

DO NOT SCALE DRAWING. UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES. TOLERANCES: ANGLES ± 0°30'. FINAL SURFACE QUALITY. REMOVE BURRS AND BREAK SHARP CORNERS.

MATERIAL: SEE PARTS LIST

FINISH: —

DRN. DATE 7 APR 71 · CHK'D. DATE 4-8-71 · ENG. DATE 4-8-71 · PROJ. ENG. DATE 4-1-71 · PROD. DATE 4/9/71

NEXT HIGHER ASSY: A ML-KL8-E-0

SCALE: NONE · SHEET OF

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: CABLE ASSEMBLY (KL8E)

SIZE: D · CODE: IA · NUMBER: 7008360-0-0 · REV: F

REVISIONS: A, B, C (7008360-00001), D (7008360-00002), E (7008360-00003), F (BC05M-00001)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY EMPellegrini DATE 8/29/72	CHECKED P. Janson DATE 8-30-72	SECTION
ENG P. Janson DATE 8/29/72	PROD J. Kelly DATE 8-31-72	ISSUED SECT.

LEGEND

D	DOCUMENT
DN	DOCUMENT CHANGE NOTICE
PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
2	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
3	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 SOFTWARE LIST	SHEET 1 OF 1	A	SL	DL11-0-4		
		DIST.				

DEC FORM NO. DEC 16-(327)-1049 N471
DRA 120

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY	E. Pellegrini	CHECKED	C. Janson
DATE	June 26, 1972	DATE	8-8-72
ENG	Paul Janson	PROD	J. Thurston
DATE	June 26, 1972	DATE	8-8-72
		SECTION	
		ISSUED SECT.	

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)	-	1	-	1	1				
2	G8000	FILTER NETWORK	0	A/R	0	A/R	A/R				
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)	1	0	1	0	0				
4	5408776	PRIORITY JUMPER LEVEL #4	1	1	1	1	1				
5	BC05-C-25	MODEM CABLE	0	1	0	1	1				
6	7008360	TTY CABLE	1	0	1	0	0				
7	-	CRYSTAL	1	1	1	1	1				
8	-	DL11 ENGINEERING DRAWINGS	1	1	1	1	1				
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL	1	1	1	1	1				
10	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				
13	H315	MODEM TEST CONNECTOR	0	0	0	0	A/R				

NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.

2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.
3. ONE H315 PER PDP11 SYSTEM
4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 CHECK LIST	SHEET 1 OF 1	A	AL	DL11-0-5	C	DL11-00005
		DIST.				

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 6-21-72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	L. Condon	8/27/73
E	CHANGE PER ECO	DL11-7	CONDON	8/74	L. Condon	9/1/74
F	CHANGE PER ECO	DL11-8	CONDON	4-75	L. Condon	4/8/75

ENG	APPD	SIZE	CODE	NUMBER	REV
Paul E. Janson		A	SP	DL11-0-2	F

DEC FORM NO DRA 107A

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.

A. OPERATION MODE:

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.

J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.

J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.

J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.

J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.

J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

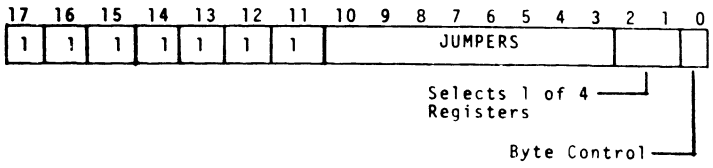
Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:



Bits 10 through 3 are controlled by jumpers A10 to A3. A jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0e2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XXØ and XX4 where XX ranges from ØØ to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A B,C,D and E use level 4, for the standard assignment or level 5-7 as specified by the customer or the documentation of an option which uses the DL11.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS	776XXØ 776XX2 776XX4 776XX6	FLOATING	BR4

Where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXXØ 77XXX2 77XXX4 77XXX6	Floating	4

Where XXX= 561 for line #1
and XXX= 617 for line #31

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

G. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6.

1050 X 960 = 10080000 = 1.008MHz.

The crystal frequency should not fall outside the range of the standard crystals. Although the above table includes only the standard DL11 crystals other values may be specified by the customer or by other documentation of an option which uses the DL11.

DEC part number for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

*Use A or C cut crystals only Do not use crystals marked NE-6D.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot AØ2 of DD11-A.
2. Wire AØ3V2 to AØ2V2.
3. Wire AØ2N2 to CXXU1 where XX is the slot location of the M7800.

Refer to diagram 1.

I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

J. DL11-B,D,E in Systems with +15V available using DD11-A
There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AØ3V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AØ3V2 to CXXU1, where XX is the slot number of the DL11. NOTE: this does not apply to DL11-A or C or DD11-B.

K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

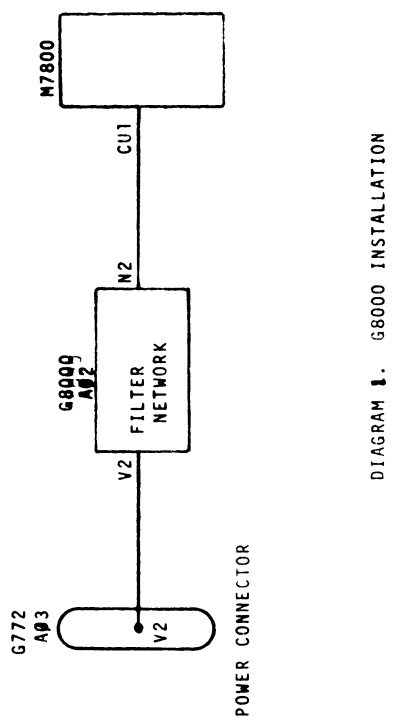
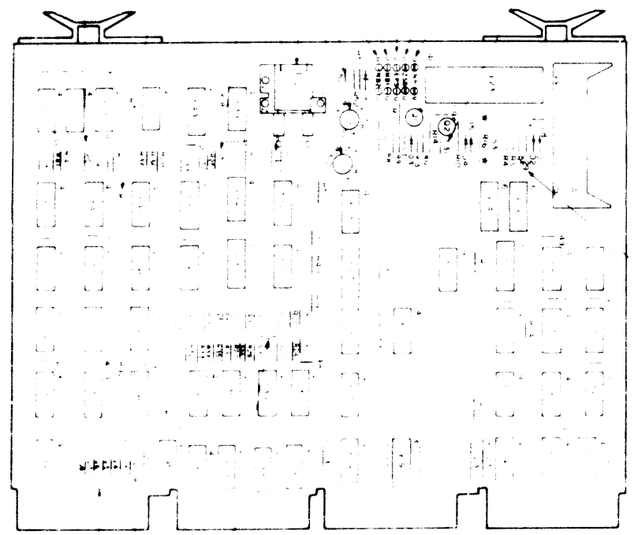


DIAGRAM 1. G8000 INSTALLATION

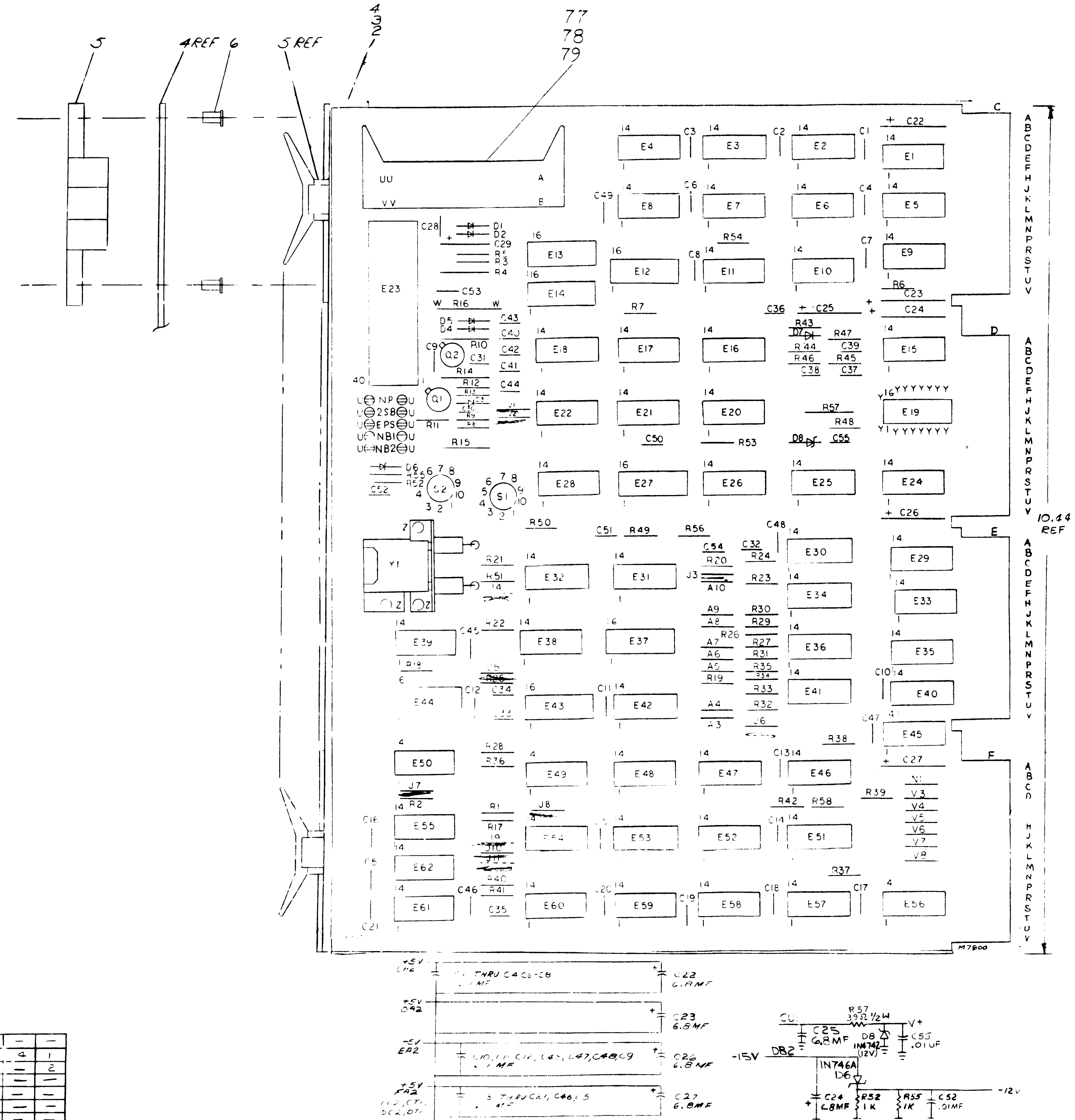


NOTES:

1. PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.
2. JUMPERS TO BE USED AT CONNECTIONS A3-A10, J1-J10, V3-V8, AND N1.
3. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).
4. DEC 8640'S WERE PHASED IN AS DEC 380 REPLACEMENTS. ANY 380 FAILURES SHOULD BE REPLACED BY 8640'S EXCEPT E28. E28 MUST BE REPLACED WITH A 7380.
5. FOR YC VERSION, C36 VALUE IS 1200PF.

PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F



PARTS LIST

QTY (YC)	QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	1	E28	IC DEC 7380	1910390	80
1	1		LATCH RIGHT	1209941-04	79
1	1		LATCH LEFT	1209941-03	78
1	1		CONNECTOR BERG	1209941-02	77
1	1		INSULATED JUMPER	9009185	76
	[illegible]	[illegible]	[illegible]	1002474	75
A/R	A/R		WIRE #2[illegible]	9107560-01	74
1	1	R57	RES 39, 1/2W, 5%	1302336	73
1	1	D8	DIODE 4742, 12V, 10%, 1W, ZENER	1109502	72
3	3		INT. WASHER #2	9006631	71
1	1	E27	IC DEC 74161	1910650	70
3	3		NUT, HEX #2	9006555	69
3	3		SCR PHL PAN HD #2-56X1/4 LG	9006001-1	68
2	2		AUGAT 8000 PG-1	1202812	67
6	6	D1-D5, D7	DIODE D664 20V 100MA	1100114	66
1	1	D6	DIODE 1N746A	1104860	65
2	2	Q1, Q2	TRANSISTOR G534D	1503409-00	64
1	1	C53	CAP 100PF 100V 5% DIPPED MICA	1000016	63
1	1	C54	CAP 560PF 100V 5% DIPPED MICA	1000025	62
2	2	C50, C51	CAP .047MF CERAMIC	1009678	61
1	1	C36	CAP 220PF 100V 5% DIPPED MICA	1000021	60
2	2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
9	7	C32, C37-C44	CAP 470PF 100V 5% DIPPED MICA	1000024	58
1	1	C31	CAP 1000PF 100V 5% DIPPED MICA	1000042	57
30	30	C1-C21, C28, [illegible]	CAP .01UF 100V 20% CERAMIC DISC	1001610-01	56
1	1	C29	CAP .47UF 35V 10% TANT	1005965	55
6	6	C22-C27	CAP 6.8 UF 35V 10% TANT	1005306	54
1	1	C33	CAP 150PF 100V 5% DIPPED MICA	1000019	53
2	2	R14, R15	RES 1.5K 1/2W 5%	1300394	52
6	6	R20, R26, R40, R48, R52, R55	RES 1K 1/4W 5%	1300365	51
1	1	R41	RES 47Ω 1/4W 5%	1300202	50
1	1	R10	RES 68Ω 1/2W 5%	1309405	49
1	1	R5	RES 8[illegible] 1/4W 5%	1301477	48
4	4	R24, R45, R46, R47	RES 100Ω 1/4W 5%	1300229	47
1	1	R11	RES 150Ω 1/4W 5%	1300250	46
2	2	R42, R58	RES 180Ω 1/4W 5%	1301322	45
2	2	R44, R53	RES [illegible] 1/4W 5%	1300271	44
1	1	R38	RES 390Ω 1/4W 5%	1300309	43
4	4	R9, R13, R43, R51	RES [illegible] 1/4W 5%	1300316	42
1	1	R4	RES 560Ω 1/2W 5%	1300338	41
1	1	R3	RES 750Ω 1/4W	1301401	40
1	1	R16	RES 750Ω 1W 5%	1302385	39
27	27	R1, R2, R6, R7, [illegible]-R22, R25, R27-R37, R39, [illegible], R50, [illegible], R54, R56	RES [illegible] 1/4W 5%	1300479	38
2	2	R8, R12	RES 1.5K 1/4W 5%	1300391	37
		E23	IC DEC UART	1910459	36
4	4	E32, E35, E61, E62	IC DEC 7474	1905547	35
3	3	E15, E36, E41	IC DEC 8242	1909712	34
3	3	E31, E49, E59	IC DEC 7408	1910155	33
2	2	E18, E21	IC MC 1489	1910323	32
		[illegible], E26	IC DEC 7490	1909057	31
	11	E1, E2, E5, E7-E9, [illegible], E30, E47, [illegible]	IC DEC 8881	1909705	30
1	1	E22	IC MC 1488	1910322	29
1	1	E43	IC DEC 74123	1910436	28
3	3	E48, E57, E52	IC DEC 74H74	1909667	27
3	3	E42, E54, E58	IC DEC 7400	1903575	26
1	1	E10	IC DEC 7413	1909989	25
2	2	E50, E53	IC DEC 7402	1909004	24
		E3, E4, [illegible], E45, E46	IC DEC 8640	1911469	23
1	1	E12	IC DEC 74153	1909937	22
1	1	E60	IC DEC 74H04	1909931	21
1	1	E25	IC DEC 7492	1909053	20
	5	E6, E16, E17, E38, E39	IC DEC 7404	1909686	19
1	1	E24	IC DEC 7493	1909054	18
1	1	E34	IC DEC 7410	1903576	17
1	1	E29	IC DEC 314	1909704	16
1	1	E37	IC DEC 7442	1910046	15
1	1	E44	IC DEC 8271	1909615	14
2	2	E13, E14	IC DEC 74175	19106[illegible]	13
1	1		BRACKET, CRYSTAL HOLDER	5302823	12
1	1		BRACKET, CRYSTAL HOLDER	5303154	11
1	1	E19	IC SOCKET	1209838	10
2	2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1210042-1	9
1	1		~~40 PIN CONNECTOR BERG~~	[illegible]	8
10	10		SPLIT LUGS	9006733	7
8	8		EYELET #GS-4-7 E.B. STIMPSON	9006732	6
4	4		HANDLE, FLIP-CHIP, MAGENTA	9008337-06	5
1	1		ETCHED CIRCUIT BOARD	5009[illegible]	4
REF	REF		MODULE ECO HISTORY	A-MH-[illegible]	3
REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-[illegible]	2
REF	REF		X-Y COORDINATE HOLE	K-CO-[illegible]	1

ETCH BOARD REV H

IC TYPE	GND	+5V	+V	-12V
DEC 74161	8	16	—	—
DEC 1488	7	—	4	1
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

SEMICONDUCTOR CONVERSION CHART

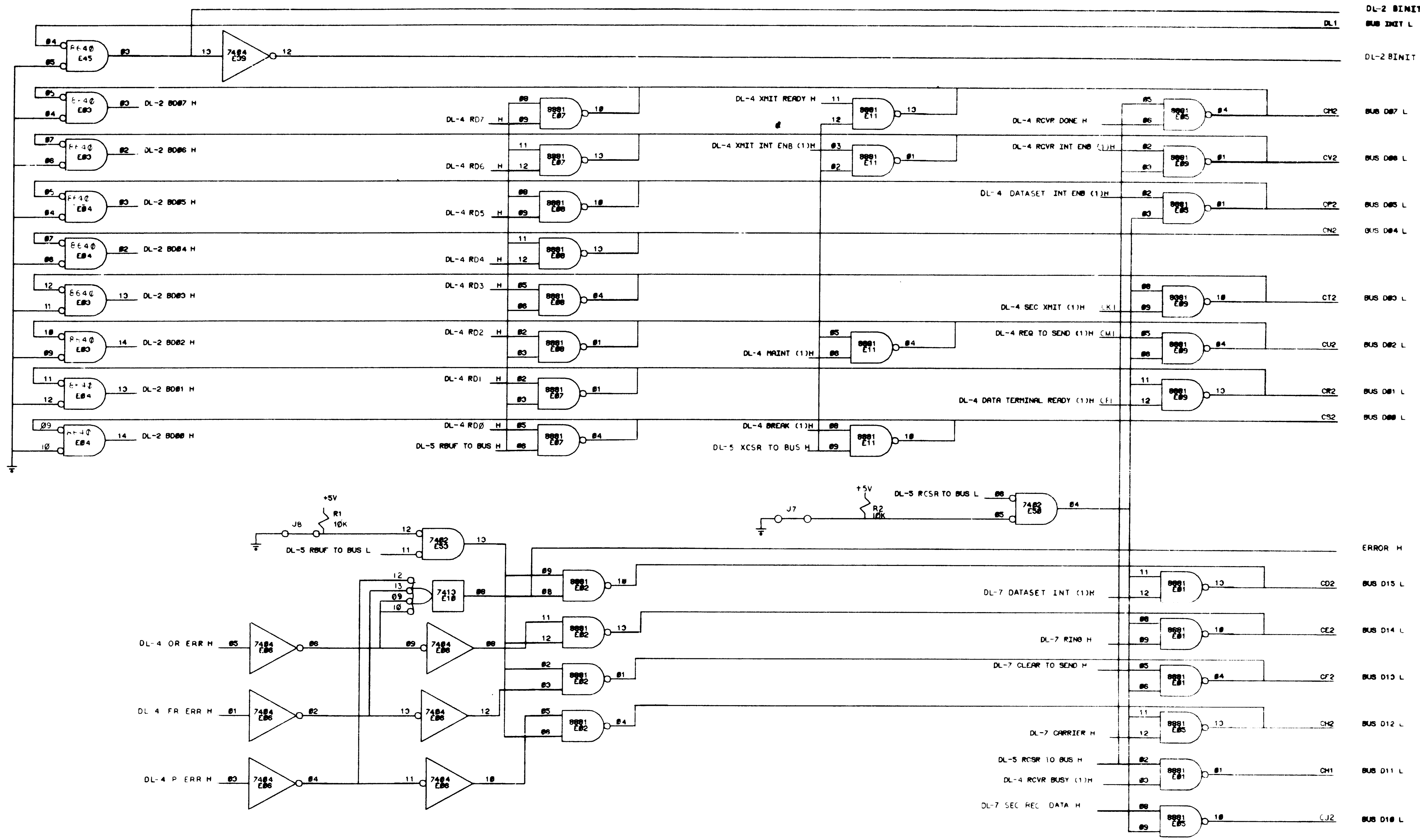
DEC NO.	EIA NO.
G534D	MPS6534
1N746A	1/4M3.3AZ
D664	1N3606

DRN. M. Pierce DATE 2/8/72
CHK'D. DATE 4-7-72
NEXT HIGHER ASSY
SHEET 1 OF 2

EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

E CS M7800-0-1 P


DL-2 BINIT H
BUS INIT L
DL-2 BINIT L
DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H
DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H
DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 REQ TO SEND (1)H
DL-4 DATA TERMINAL READY (1)H
BUS D07 L
BUS D06 L
BUS D05 L
BUS D04 L
BUS D03 L
BUS D02 L
BUS D01 L
BUS D00 L
DL-5 RCSR TO BUS L
DL-5 RBUF TO BUS L
ERROR H
DL-4 OR ERR H
DL 4 FR ERR H
DL-4 P ERR H
DL-7 DATASET INT (1)H
DL-7 RING H
DL-7 CLEAR TO SEND H
DL-7 CARRIER H
DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H
DL-7 SEC REC DATA H
BUS D15 L
BUS D14 L
BUS D13 L
BUS D12 L
BUS D11 L
BUS D10 L

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.
DL11	PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS: .XXX = .005, .XX = .02, .X = .1
ANGLES: ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—/—
FINISH —/—/—

DRN. B. Pe... DATE 3-20-72
CHK'D. ... DATE 4-5-72
ENG. ... DATE ...
PROD. ENG. ... DATE 4-27-72
DATE 4-27-72

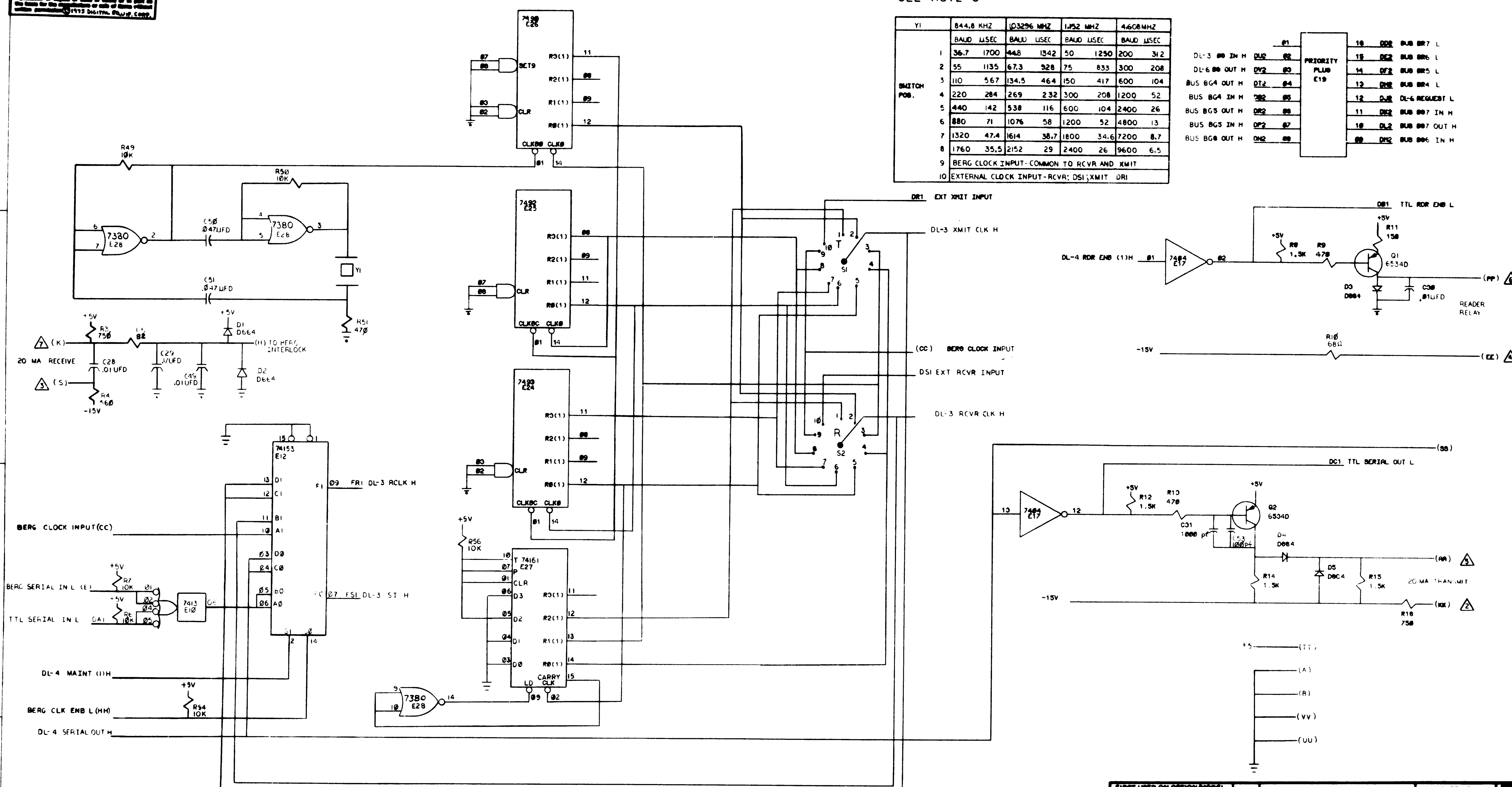
NEXT HIGHER ASSY.
SCALE
SHEET 2 OF 7

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE D CODE CS NUMBER M7800-0-1 REV. P

REVISIONS: CHK. | CHANGE NO. | REV.



SEE NOTE 3

Y1		844.8 KHZ		1.03296 MHZ		1.152 MHZ		4.608 MHZ	
		BAUD	µSEC	BAUD	µSEC	BAUD	µSEC	BAUD	µSEC
SWITCH POS.	1	36.7	1700	44.8	1342	50	1250	200	312
	2	55	1135	67.3	928	75	833	300	208
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	208	1200	52
	5	440	142	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	13
	7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
	8	1760	35.5	2152	29	2400	26	9600	6.5
	9	BERG CLOCK INPUT- COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT-RCVR; DS1; XMIT DR1							

NOTES:

1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD DL11 CRYSTALS OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION OF AN OPTION WHICH USES THE DL11.

FIRST USED ON OPTION/MODEL: DL11

QTY. | DESCRIPTION | PART NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

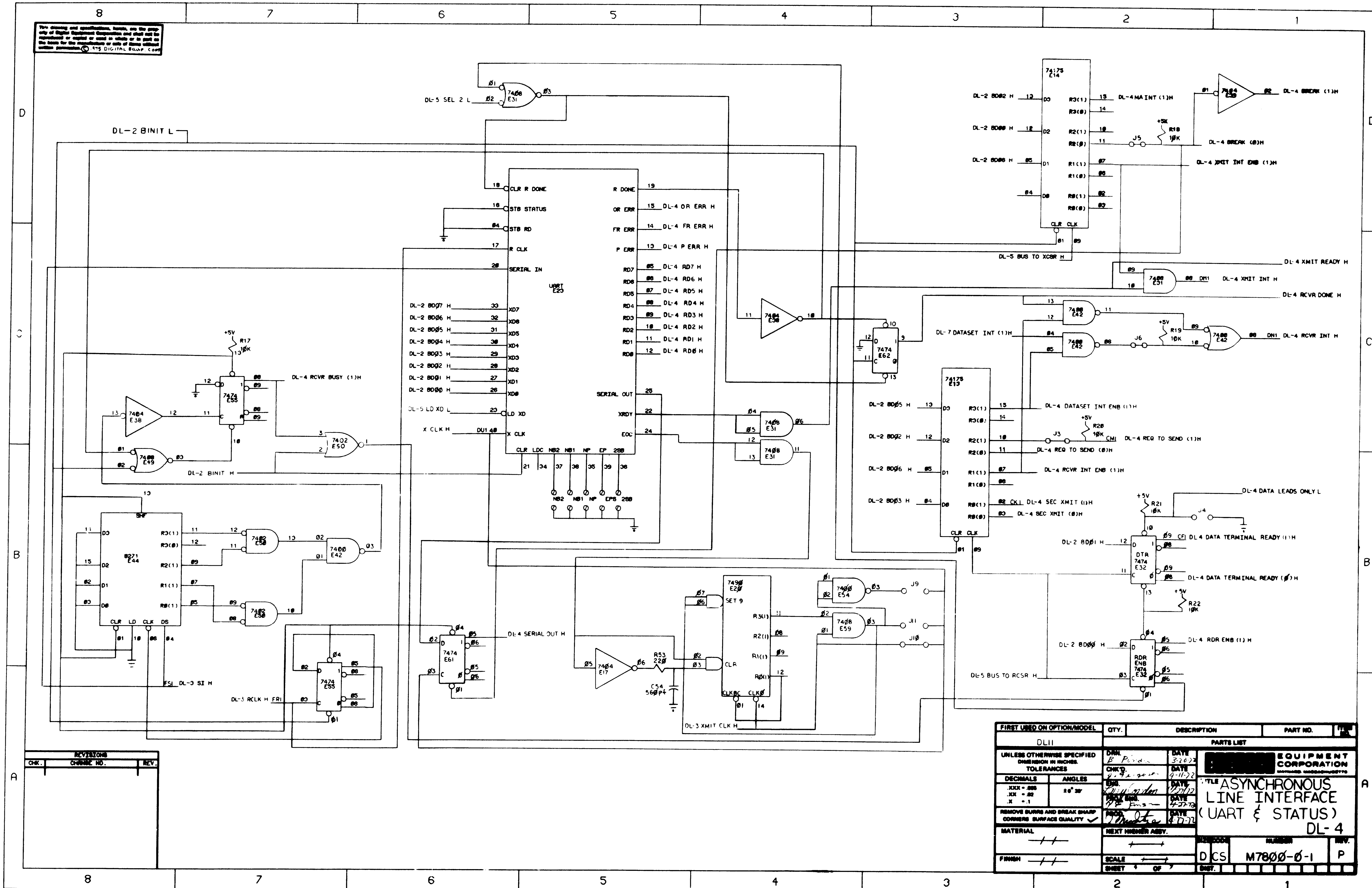
DR. B Pirie DATE 3-20-72
CHK'D. DATE 4-5-72
DATE 4-27-72
DATE 4-27-72

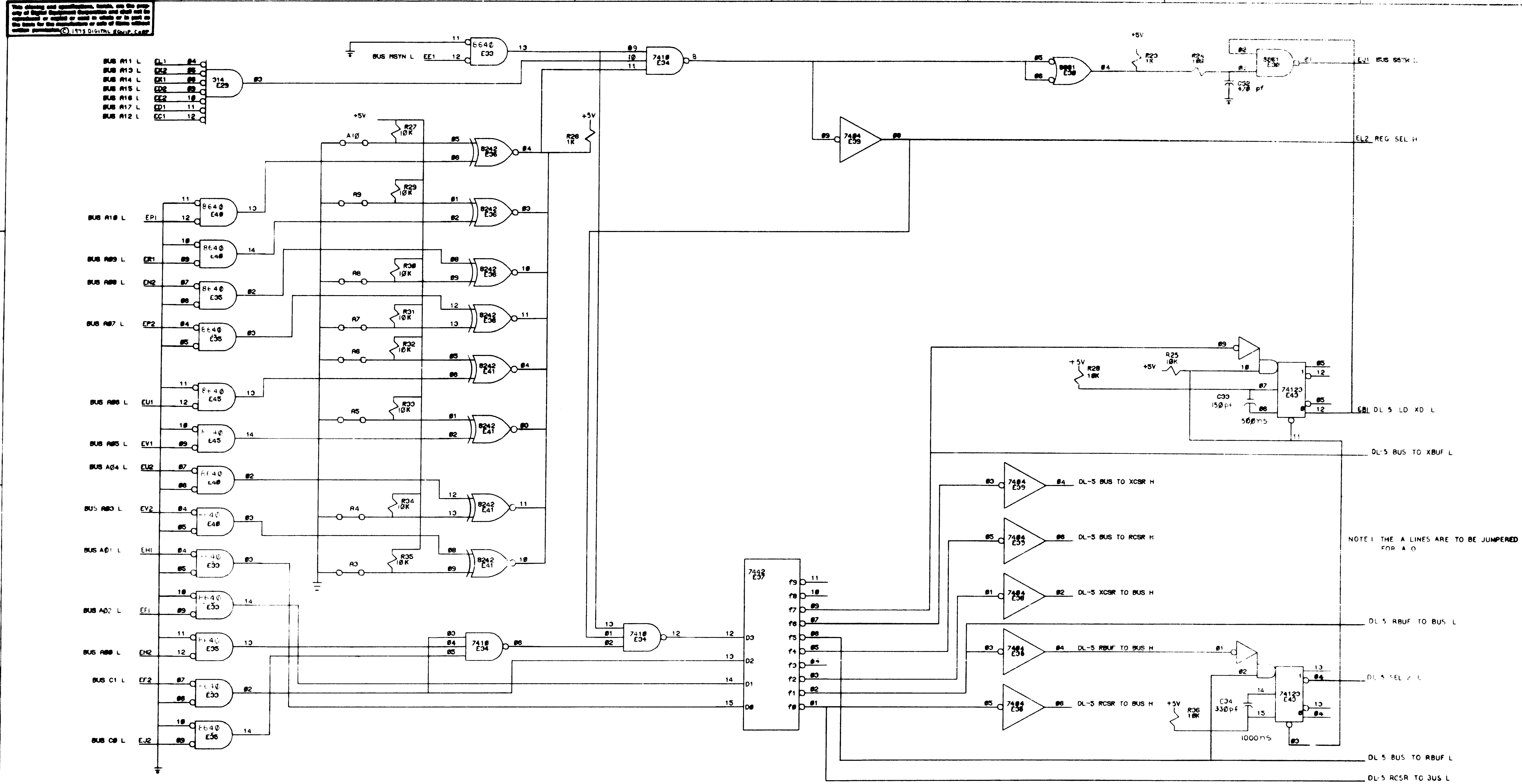
[redacted] EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

D CS M7800-0-1 REV. P

REVISIONS


ASYNCHRONOUS LINE INTERFACE (UART & STATUS)
DL-4
M7800-0-1
DL11
EQUIPMENT CORPORATION
UART E23
DL-2 BINIT L
DL-5 SEL 2 L
DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-4 RCVR BUSY (1)H
DL-4 SERIAL OUT H
DL-4 XMIT READY H
DL-4 XMIT INT H
DL-4 RCVR DONE H
DL-4 RCVR INT H
DL-4 BREAK (1)H
DL-4 DATA LEADS ONLY L
DL-4 DATA TERMINAL READY (1)H
DL-4 RDR ENB (1) H
DL-5 BUS TO RCSR H
DL-5 BUS TO XCSR H
DL-3 XMIT CLK H
DL-3 RCLK H
DL-3 SI H



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.
DL11		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS .XXX = .005 .XX = .02 .X = .1 — ANGLES ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—

FINISH —/—

NEXT HIGHER ASSY.

SCALE

SHEET 1 OF 7

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5

SIZE D CODE CS NUMBER M7800-0-1 REV. P