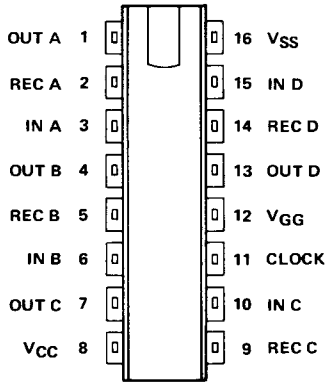
# TMS 3120 JC, NC; TMS 3121 JC, NC
# QUADRUPLE 80-, 64-BIT STATIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512267, MAY 1975

- DC to 2.5-MHz Operation
- Static Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- Push-Pull Output Buffers
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- Low-Threshold MOS Technology

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)






## description

The TMS 3120 and TMS 3121 are quad 80-bit and quad 64-bit shift registers with independent inputs, outputs, and recirculate controls for each register. A single-phase clock is common to all registers. The clock and data inputs can be driven from Series 74 TTL circuits and the push-pull output buffers can drive one TTL load or low-level MOS loads without external pull-up resistors.

Cross-coupled inverters (flip-flops) are employed to implement each bit storage location. This static design allows input data rates from dc to 2.5 MHz and long-term data storage.

P-channel enhancement-type low-threshold processing has been employed to reduce power dissipation and provide simple interface with bipolar circuits.

The TMS 3120 and TMS 3121 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

## applications

The TMS 3120 can be used in card punch, key-to-tape, key-to-disk, printer, and CRT display equipment for both 40- and 80-column applications. The TMS 3121 is used in general purpose buffer memories.

## operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock. Input data must be set up a minimum time before the high-to-low clock transition and must be held for a minimum time after that transition. For long term data storage, the clock must be maintained low, and in this mode the recirculate and data input levels may change without affecting the data output levels.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the output and the data input is inhibited.



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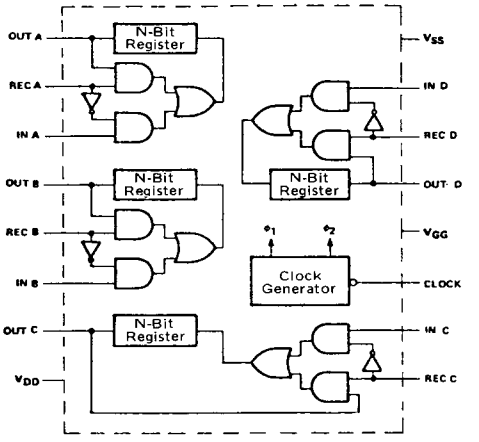
## functional block diagram

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

| | |
|---|---|
| Supply voltage, $V_{DD}$ (see Note 1) | −20 V to 0.3 V |
| Supply voltage, $V_{GG}$ (see Note 1) | −20 V to 0.3 V |
| Clock input voltage (see Note 1) | −20 V to 0.3 V |
| Data input voltage (see Note 1) | −20 V to 0.3 V |
| Operating free-air temperature range | −25°C to 85°C |
| Storage temperature range | −55°C to 150°C |

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, $V_{SS}$ (substrate). Throughout the remainder of this data sheet voltage values are with respect to $V_{DD}$.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 0 | | V |
| Supply voltage, $V_{GG}$ | −11 | −12 | −13 | V |
| Supply voltage, $V_{SS}$ | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | $V_{SS}$ −1.6 | | | V |
| High-level clock input voltage, $V_{IH(\phi)}$ | $V_{SS}$ −1.6 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Low-level clock input voltage, $V_{IL(\phi)}$ | | | 0.8 | V |
| Clock pulse transition time, low-to-high-level, $t_{TLH(\phi)}$ | | | 10 | μs |
| Clock pulse transition time, high-to-low-level, $t_{THL(\phi)}$ | | | 10 | μs |
| Pulse width, clock high, $t_{w(\phi H)}$ | 200 | | 100000 | ns |
| Pulse width, clock low, $t_{w(\phi L)}$ | 200 | | ∞ | ns |
| Data setup time, $t_{su(da)}$ | 190 | | | ns |
| Recirculate setup time, $t_{su(rec)}$ | 190 | | | ns |
| Data hold time, $t_{h(da)}$ | 90 | | | ns |
| Recirculate hold time, $t_{h(rec)}$ | 90 | | | ns |
| Clock frequency, $f_{\phi}$ (see Note 2) | 0 | | 2.5 | MHz |
| Operating free-air temperature, $T_A$ | −25 | | 85 | °C |

NOTE 2: For cascading, data input frequency = 2 MHz maximum.



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## electrical characteristics under nominal operating conditions, $T_A$ = −25°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 100 μA | $V_{SS}$ −1 | $V_{SS}$ −0.5 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.6 mA | | 0.2 | 0.4 | V |
| $I_I$ | Input current (all inputs) | $V_I$ = 0 | | | −0.1 | μA |
| $I_{GG}$ | Supply current from $V_{GG}$ | Load = 1 TTL gate (see Note 3) f = 1 MHz, $T_A$ = 25°C | | −10 | −15 | mA |
| $I_{SS}$ | Supply current from $V_{SS}$ | Load = 1 TTL gate (see Note 3) f = 1 MHz, $T_A$ = 25°C | | 30 | 35 | mA |
| $P_D$ | Power dissipation | Load = 1 TTL gate (see Note 3) f = 1 MHz, $T_A$ = 25°C | | | 355 | mW |
| $C_i$ | Input capacitance, all inputs except clock | $V_I$ = $V_{SS}$, f = 1 MHz | | 3.5 | 5 | pF |
| $C_{i(\phi)}$ | Clock input capacitance | $V_{I(\phi)}$ = $V_{SS}$, f = 1 MHz | | 3.5 | 5 | pF |

†All typical values are at $T_A$ = 25°C.

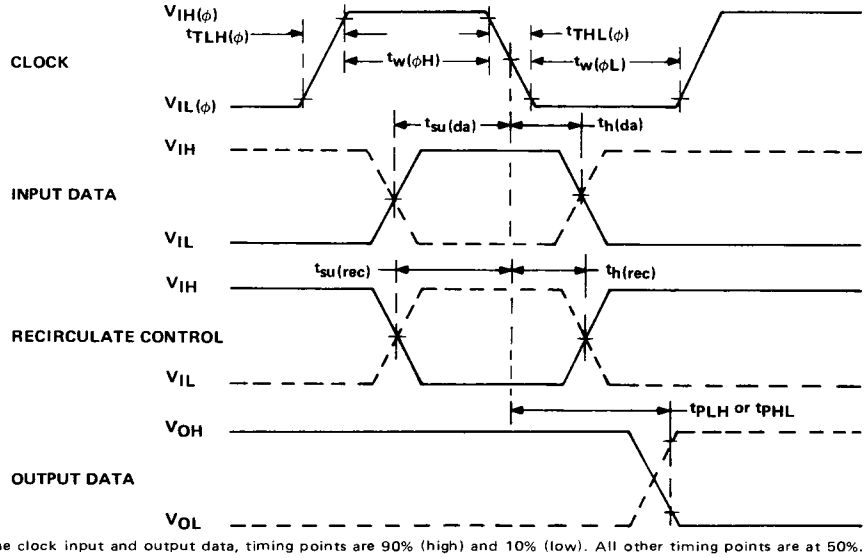
NOTE 3: For test purposes, a TTL load is simulated by a load of 2.7 kΩ and 20 pF between the output and $V_{SS}$.

## switching characteristics under nominal operating conditions, $T_A$ = −25°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from clock | 1 Series 74 TTL Load + 10 pF (see Note 4) | 100 | 400 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clock | | 100 | 400 | ns |
| $t_{PLH}$ | Propagation delay time, high-to-low-level output from clock | $R_L$ = 10 MΩ, $C_L$ = 10 pF (MOS Load), (see Note 4) | 100 | 300 | ns |
| $t_{PHL}$ | Propagation delay time, low-to-high-level output from clock | | 100 | 300 | ns |

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and $V_{SS}$.

## voltage waveforms




NOTE: For the clock input and output data, timing points are 90% (high) and 10% (low). All other timing points are at 50%.



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