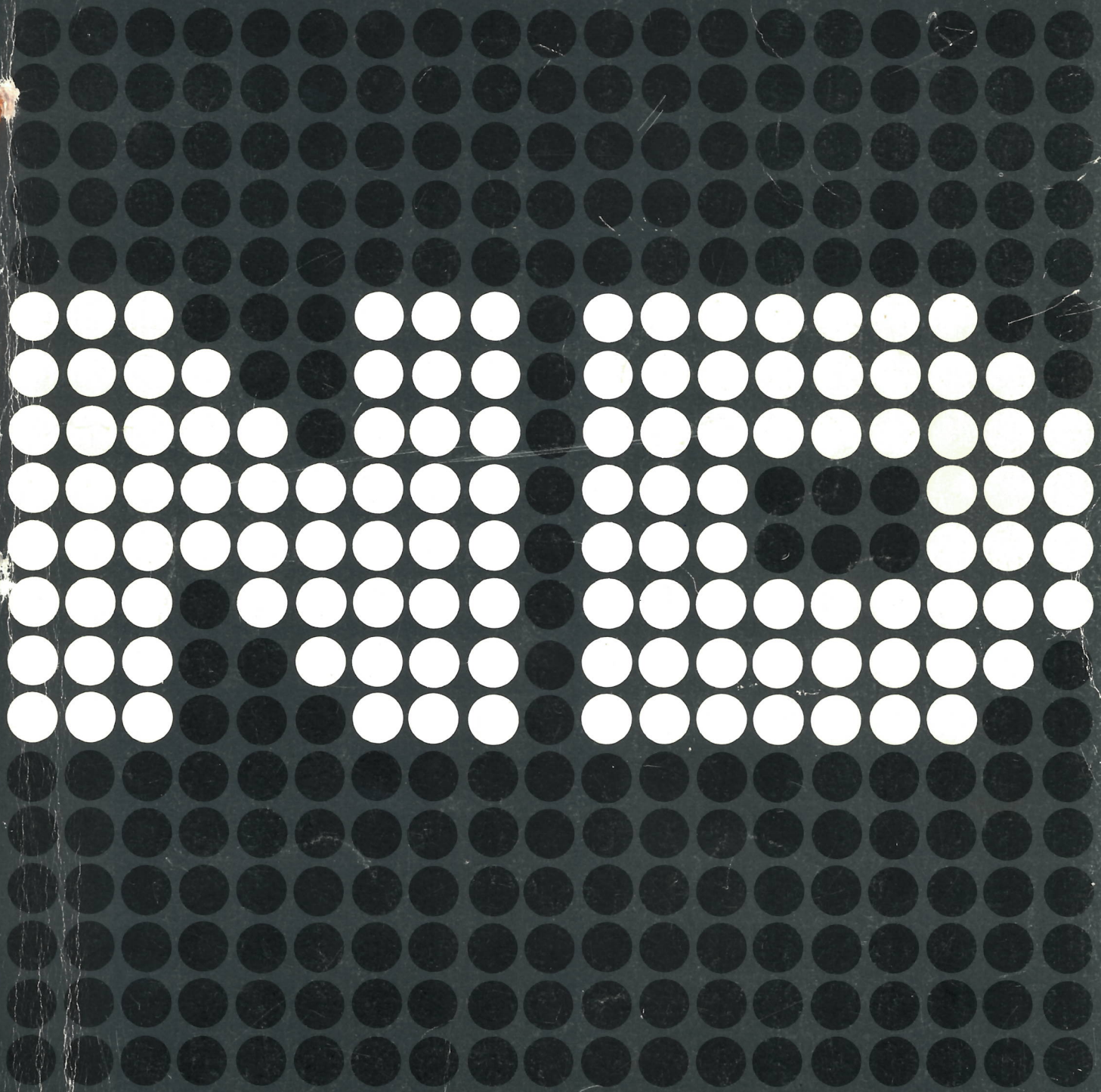
NORD 10/S
INPUT/OUTPUT SYSTEM

NORSK DATA A.S



NORD 10/S
INPUT/OUTPUT SYSTEM

REVISION RECORD

Revision	Notes
05/78	Original Printing

NORD-10/S Input/Output System
Publ.No.ND-06.012.01

NORSK DATA A.S.
Lørenveien 57, Postboks 163 Økern, Oslo 5, Norway

TABLE OF CONTENTS

+ + +

1 NORD-10/S INPUT/OUTPUT SYSTEM

After the introduction this chapter will cover the different ways of Input/Output communication and how this is implemented in NORD 10/S.

1.1 *INTRODUCTION*

For data entering or leaving the general-purpose 16 bits computer NORD-10/S there is two possibilities:

1. Via a Programmed Input/Output-interface
2. Via a Direct Memory-Access interface

Both interface types serve the following function:

- Syncronize the speed of the CPU and the device.
- Convert the data to a suitable format before entering or after leaving the physical device.

1. PROGRAMMED INPUT/OUTPUT INTERFACE (PIO)

The PIO interface is, with a few exceptions, made of one card module with dimensions given in Appendix E. One card for each device, occupies one slot in the I/O rack.

All data and control information is exchanged between registers in the interface and the accumulator or the A-register in the CPU register block. Programmed I/O interfaces are used for all slow serial or byte oriented peripheral devices. Typical: Tape-reader, Card-reader, Line printer, Display, Modem. The data transfer between the A-register and the interface is programmed. A separate Input-Output Execute instruction (IOX) is required to exchange data between the A-register and interface registers. The register-address is given by the 11 lower bits of the IOX-instruction.

The exchanged data may be:

1. Data (byte or word)
2. Control information
3. Status information

2. DIRECT MEMORY ACCESS INTERFACE (DMA)

The Direct Memory-Access interface normally consists of 4 to 12 cards located in the I/O rack. The DMA interface transfers blocks of data:

- Directly to/from the multiport memory via one separate port.
- To/from the local memory in the CPU-rack.
- To/from the multiport memory via the CPU port.

The two last transfers are based on CPU cycle stealing, while the first transfer takes place simultaneously with the CPU if the CPU and the DMA are accessing different banks. Typical DMA devices are DISKS, DRUMS, PLOTTERS and MAG-TAPES.

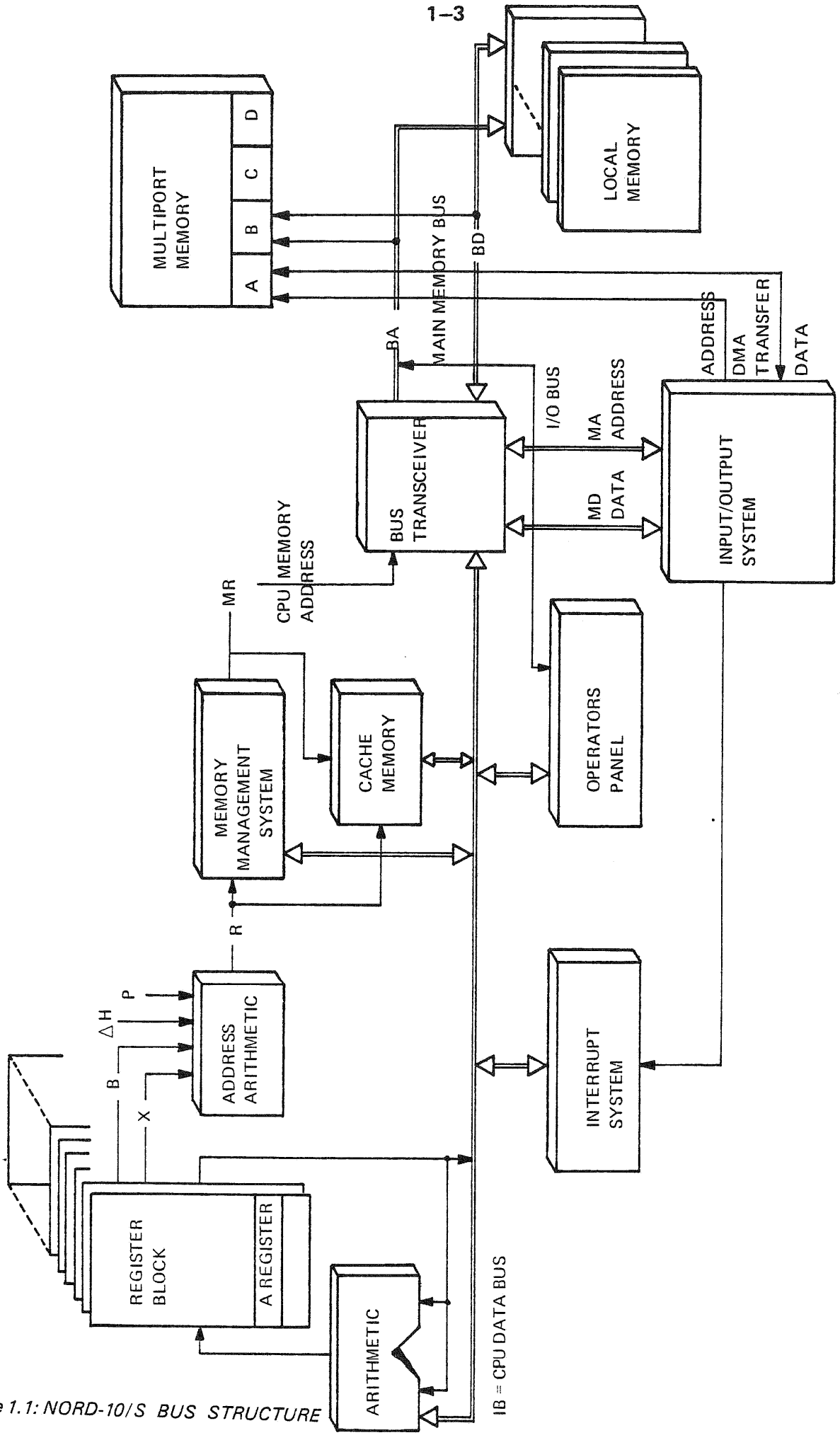


Figure 1.1: NORD-10/S BUS STRUCTURE

ND-06.012.01

1.2 *NORD-10/S I/O BUS-ARCHITECTURE*

I/O communication between the CPU/MEMORY and I/O rack B or C is carried out over the MAIN I/O BUS. (Refer to figure 1.2) The bus may be subdivided into three parts:

- Data Bus (MD)
- Address Bus (MA)
- Control Lines

All signals in the MAIN I/O BUS are carried on differential lines.

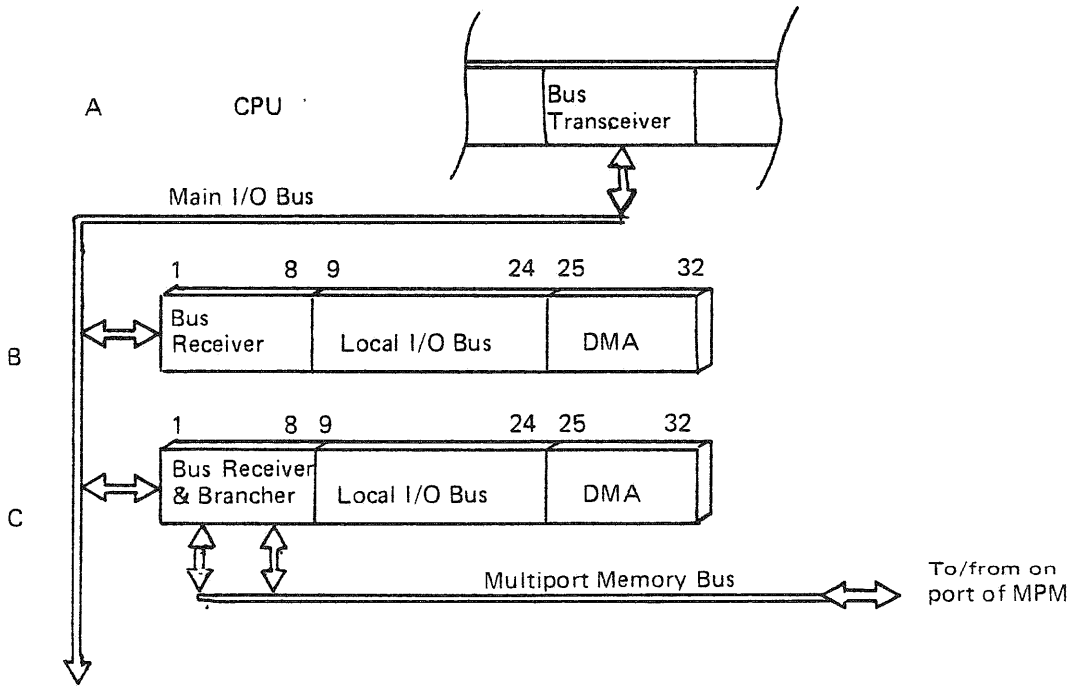


Figure 1.2: I/O ARCHITECTURE, BLOCK DIAGRAM

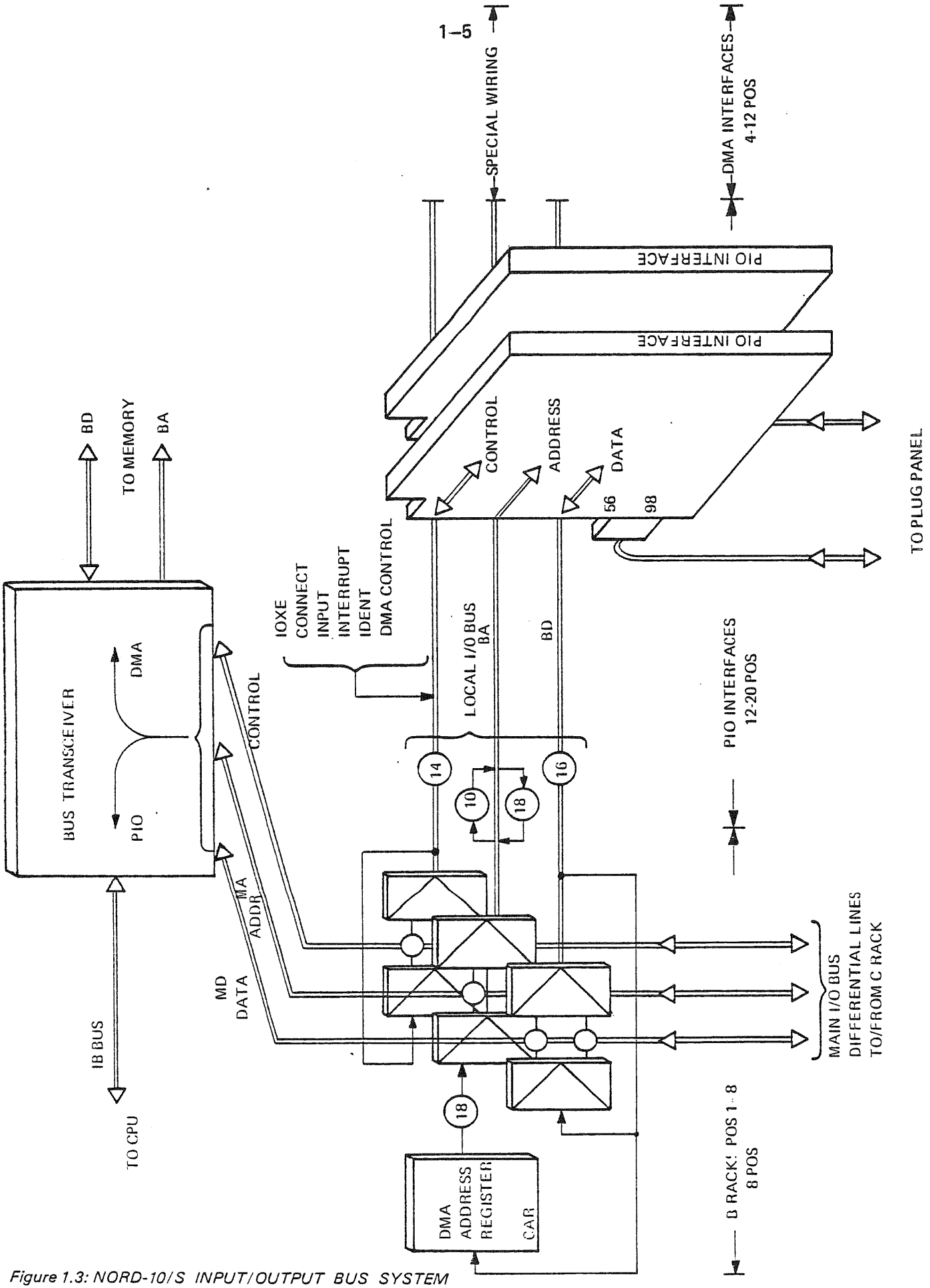


Figure 1.3: NORD-10/S INPUT/OUTPUT BUS SYSTEM

1.2.1 *BUS TRANSCEIVER:*

The BUS TRANSCEIVER which occupies 3 slots between the CPU and the local memory in the A-rack has the following main functions when communicating with a PIO interface (A) and a DMA interface (B):

A:

Establishes the communication between the addressed device interface register and the A-register.

The data lines MD will either be equal to the A-register if an output operation or equal to the addressed device-interface register if an input operation. Data is transferred to/from the A-register via the CPU data-bus IB.

The address given in the 11 lower bits in the Instruction-Register (IR) is routed out on the address lines MA.

B:

The BUS-TRANSCEIVER administrates the usage of the memory address bus BA and the memory data bus BD. These busses are connected either to the local memory in the A-rack or to one port in the multiport memory, or both.

Two sources are supplying data and address to the BUS TRANSCEIVER modules:

- CPU with the physical memory address as output of the paging system and data (if MEMORY-WRITE) on the CPU-data-bus or Information-bus IB.
- DMA with the memory-address on the MA-lines from a memory address register (CAR) and data from the interface on the MD lines.

During a DMA transfer the CPU is allowed to use the IB bus. This implies that CPU can fetch instructions and data from the CACHE memory independent of the DMA transfer. If a CPU and a DMA memory request should appear simultaneously, the BD and BA lines will be allocated to the DMA-transfer. The DMA requests have higher priority than the CPU request.

1.2.2 *BUS RECEIVER/BRANCHER. (8 left-most positions in the I/O rack)*

The modules installed here are called BUS-RECEIVER when establishing the communication between the Local I/O bus in the rack and the Main I/O bus.

The modules are called BUS-BRANCHER when communicating with one port in the multiport-memory during a DMA transfer.

1.3 *I/O CARD CRATE- Physical Layout.*

The 8 left-most positions in an I/O card crate are assigned for modules converting the Main I/O bus to a local tristate-bus. Three empty positions are set off for Main-bus expansion to the next I/O rack via plugs in the backwiring.

The right-most positions in the I/O rack are set-off for DMA interfaces.

Typical DMA interfaces and interface modules are listed below:

Interface:	*No. of Modules:*	*Remarks:*
DRUM Vermont)	8	1 DRUM
CARTRIDGE-DISK	8	Daisy-chain up to 4 DISK-DRIVES
PERTEC MAG-TAPE	4	Communicate with up to 2 Formatters.4 MAG-TAPE Units pr. formatter.
BIG-DISK(33 or 66 M-Bytes)	12	Communicate with up to 6 DISK-DRIVES. One module per drive.

In addition to the modules listed, the DMA interface is represented in the local I/O bus with one module (the BUS-CONTROL 1022 or 1155). (1155 module is used in the BIG-DISK interface with ERROR-CORRECTION).

The positions between the DMA interface and the BUS-RECEIVER/BRANCHER are assigned for a local I/O bus where PIO interfaces can be placed in any order.

1.3.1 *I/O CARD-CRATE Expansion (Refer to Figure 1.4)*

Only two I/O card crates (Band C) are installed in the CPU cabinet, for more I/O card crates the following is possible:

For ND:

The Main I/O bus is fed to three plugs in the plug panel via the empty expansion position in the C-rack.

For the Customer:

The local I/O bus is buffered and differentiated on three modules in the local I/O BUS, and fed to three plugs in the plug-panel.

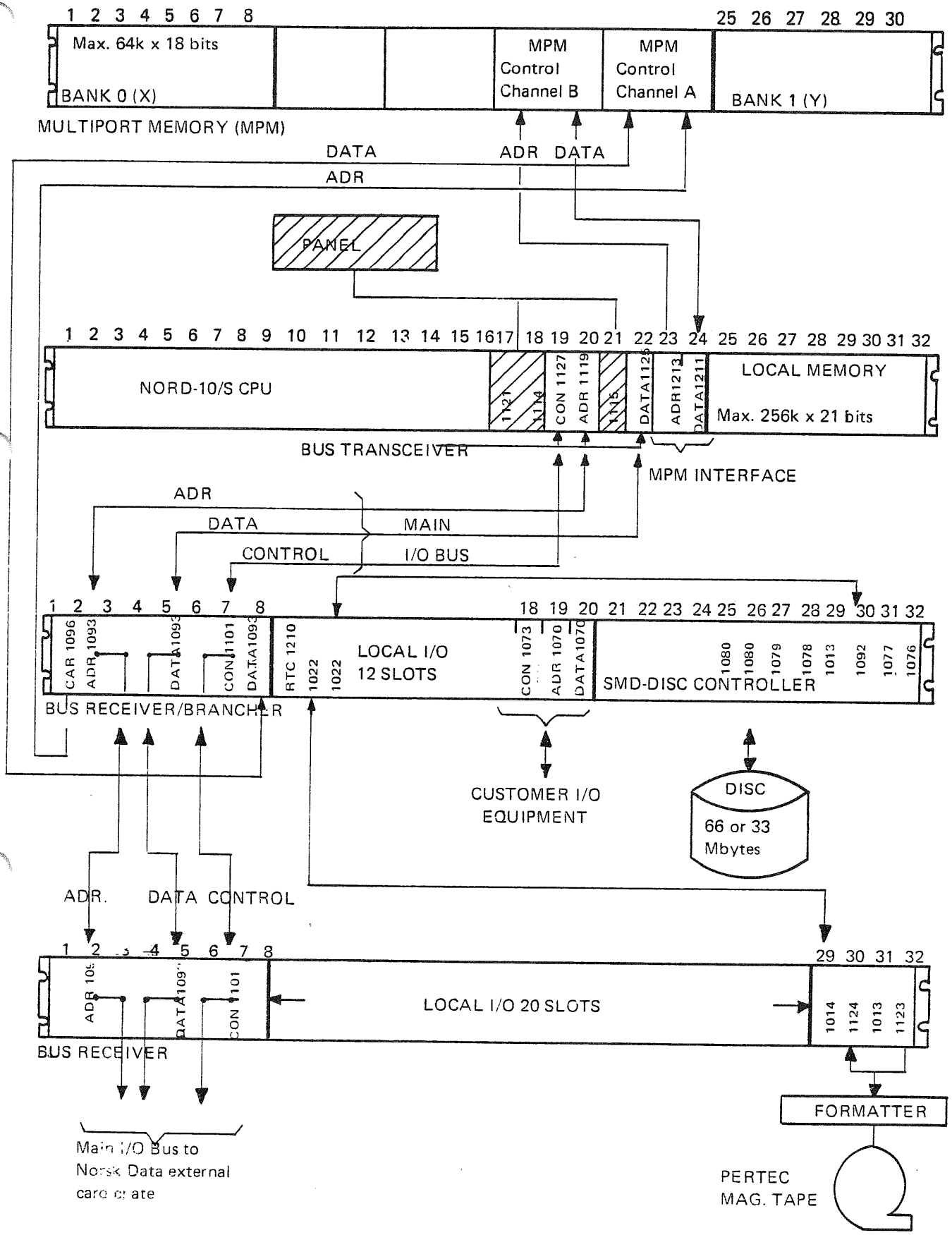


Figure 1.4: NORD-10/S EXAMPLE OF I/O CONFIGURATION

2. PROGRAMMED INPUT/OUTPUT (PIO)

This chapter will deal with the programmed input/output interface and further usage and implementation of the IOX instruction.

On each interface module there are at least three registers:

1- Data Register

1- Control Word Register

1- Status-Register

These registers are sufficient for a one way data flow interface. For a two-way data flow interface, communicating both ways as a teletype or modem, twice the amount of registers is necessary, 3 registers for output and 3 registers for input.

Data Register:

There are two kinds of data registers; a register operating as a latch (in use on interfaces for parallel-data transfer, eg., tape-reader,tape punch, card reader, line printer).

or

Serial input/parallel output register or parallel input/serial output register, in use on interfaces for serial-data transfer, eg., teletype, display, modem.

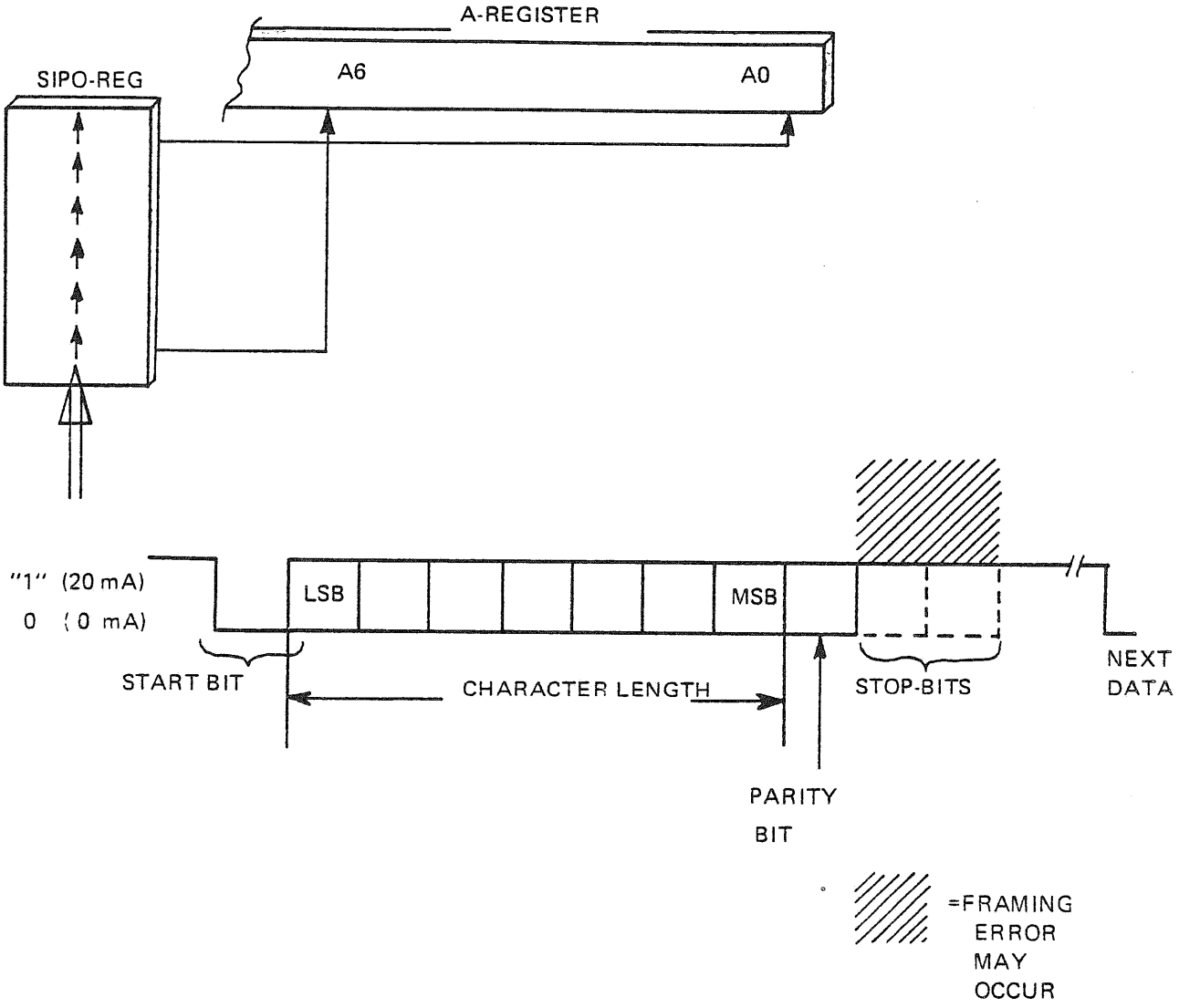


Figure 2.1: ASC II SERIAL FORMAT

Control Word Register:

—Activate device
Feed card, advance paper-tape to next sprocket, print character if Bit 2 is set.

—Set mode of operation
Test mode if Bit 3 is set

—Enables for interrupt: Bit 0 and 1

—Set character length, number of stop bits and parity on teletype and modem interfaces: Bit 11 to 14

Status Register:

—Inform the CPU when the data is ready if input and data buffer are empty of output: Bit 3

—The quality of the data-transfer is given in Bit 4

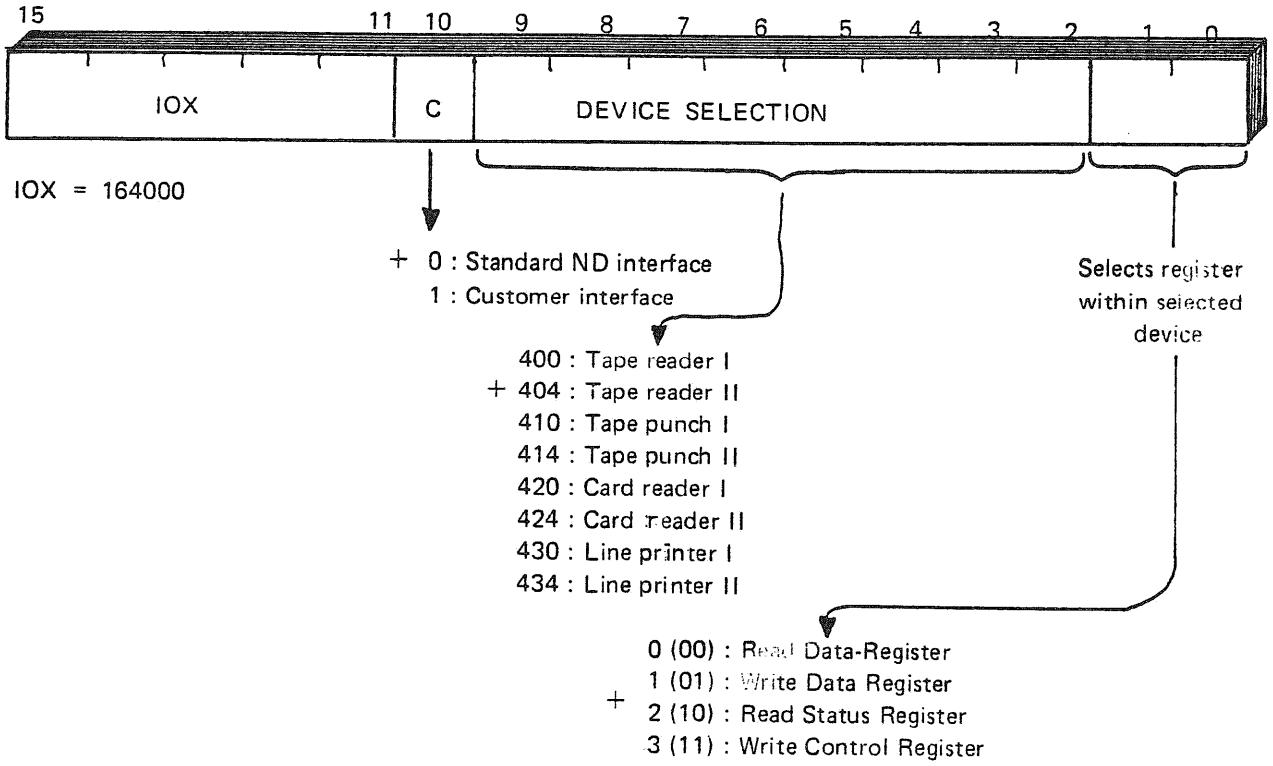
—The interrupt enabled can be examined in Bit 0 and 1

The Standard ND format of the Control-Word and Status Register is given in chapter 2.4.

PIO Interface Register Addressing:

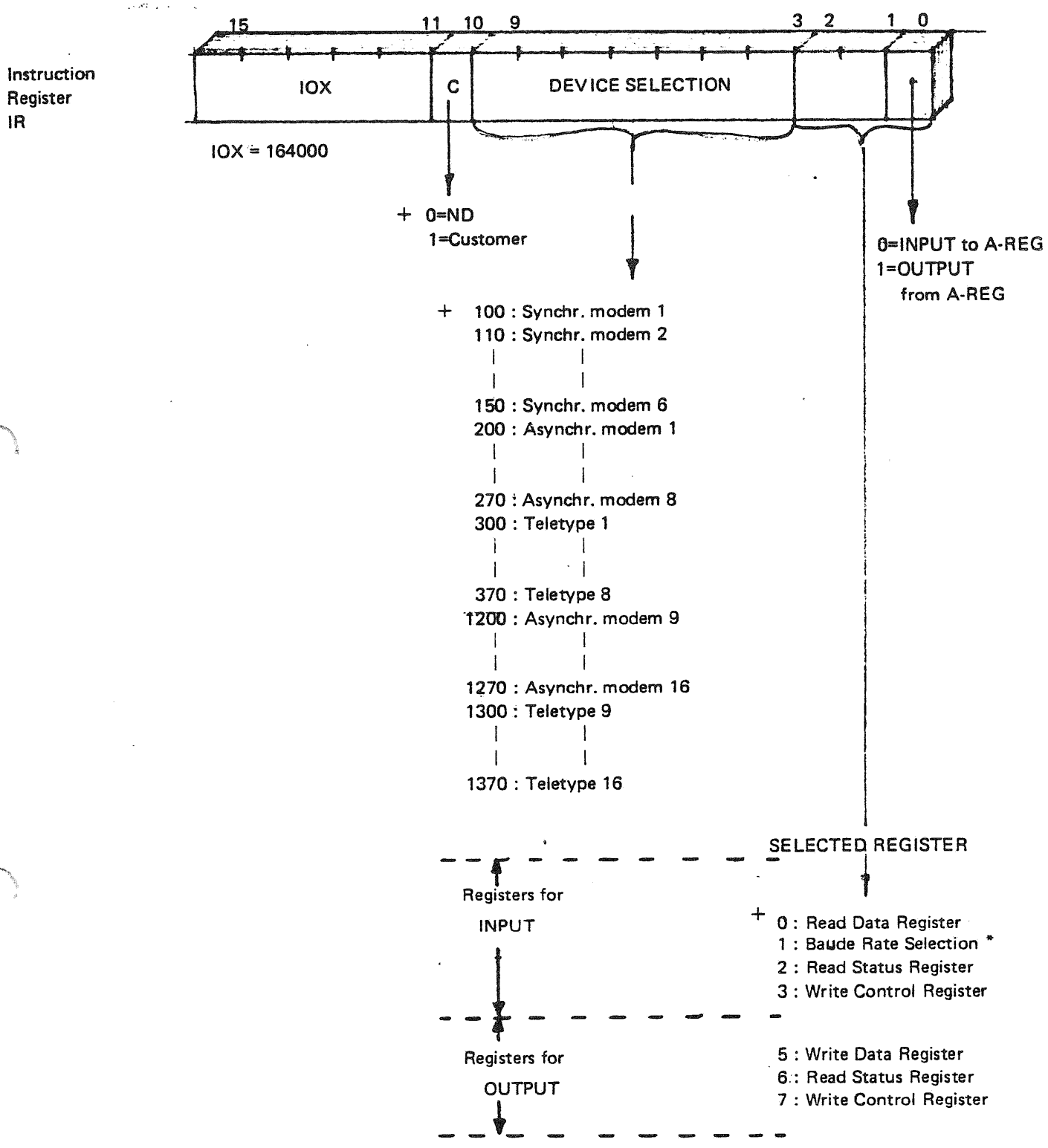
Each interface register is identified with its address. The address is given in the 11 lower bits of the Instruction-Register executing an IOX-instruction. A maximum of 2^{11} i.e. 3777_8 or 2048_{10} registers may be specified. Half of these addresses are used for standard ND interfaces while the second half are assigned for customer designed interfaces. 0-1777 = ND and 2000-3777 = Customer.

Different device-interfaces will require a different number of registers. One-way devices will usually require at least three different IOX-instructions (addresses), while two-ways and more complex interfaces as the DMA interfaces may need up to 8 registers addressed by 8 IOX instructions. The device addresses for a one way interface are in increments of four. Four device addresses per interface where the fourth register is normally a data register used for test purposes. Writeable for test pattern if input device and readable for test pattern if output device.



EX: Read Card Reader Status Register = 164422

Figure 2.1.1: IR-REGISTER DURING AN IOX INSTRUCTION TRANSFERRING DATA TO/FROM A ONE-WAY DEVICE REGISTER



* Datarate selection possible on:

- 4 ASYNC CURRENT LOOP INTERFACE 1122
- 2 ASYNC MODEM INTERFACE 1147
TERMINAL BUFFER 1095

Figure 2.1.2: TWO WAY DEVICE REGISTERS

2.1 *THE INTERFACE AND THE IOX-INSTRUCTION*

While executing, an IOX instruction the 11 lower bits of the IR-register are enabled to the address-bus (main and local). On each interface module the DEVICE SELECTION address bits, bits 2-9, if one-way and bits 3-9 if two-ways interface are compared against the address of the module. (Refer to figure 2.2).

These address bits on the module can either be given by straps or by switches. When the input to the comparator are equal (in pairs) the device address is recognized and a DEVICE EQUAL signal is generated. This signal activates the decoder, decoding the 2 or 3 least significant address-bits (BAO-2) selecting the proper register within the interface.

OUTPUT operation: (BAO = 1)

During an output operation (Ex.: IOX LOAD CONTROL WORD-REGISTER or IOX WRITE DATA REGISTER) the data on the data bus BD equal to the A-register is clocked into the proper register. The CONNECT signal can now be returned to CPU.

INPUT operation: (BAO = 0)

The register control signals from the decoder active during an INPUT-operation will:

- Select/enable the proper register out on the BD data-bus
- Be OR'ed together generating the INPUT-signal

When the input data is enabled out on the BD-bus, the CONNECT signal can be returned to the CPU.

The INPUT signal will enable the I/O Data-Bus on to the CPU data bus IB in the BUS TRANSCEIVER. The returned CONNECT signal will generate a clock signal to the H-register clocking the IB-bus. The H-register is then transferred to the A-register via the arithmetic.

As shown in figure 2.3, it may be possible to perform both an output and an input transfer on the same IOX instruction. This is done by delaying the CONNECT and INPUT signal until the BD-bus is strobed by the device. Standard ND produced interfaces are not using this feature, therefore, after an IOX input operation, the A-register will be a copy of the selected register.

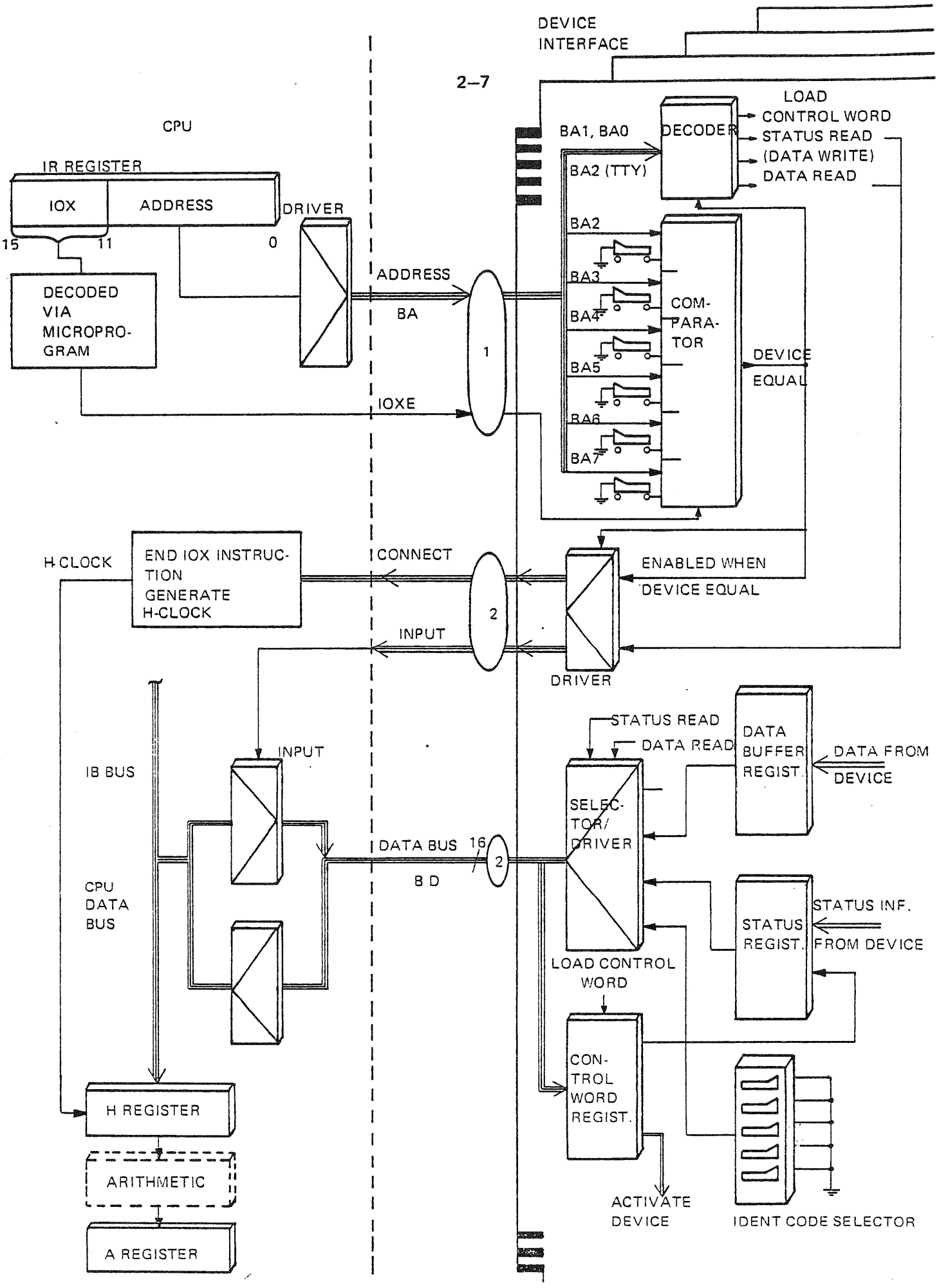
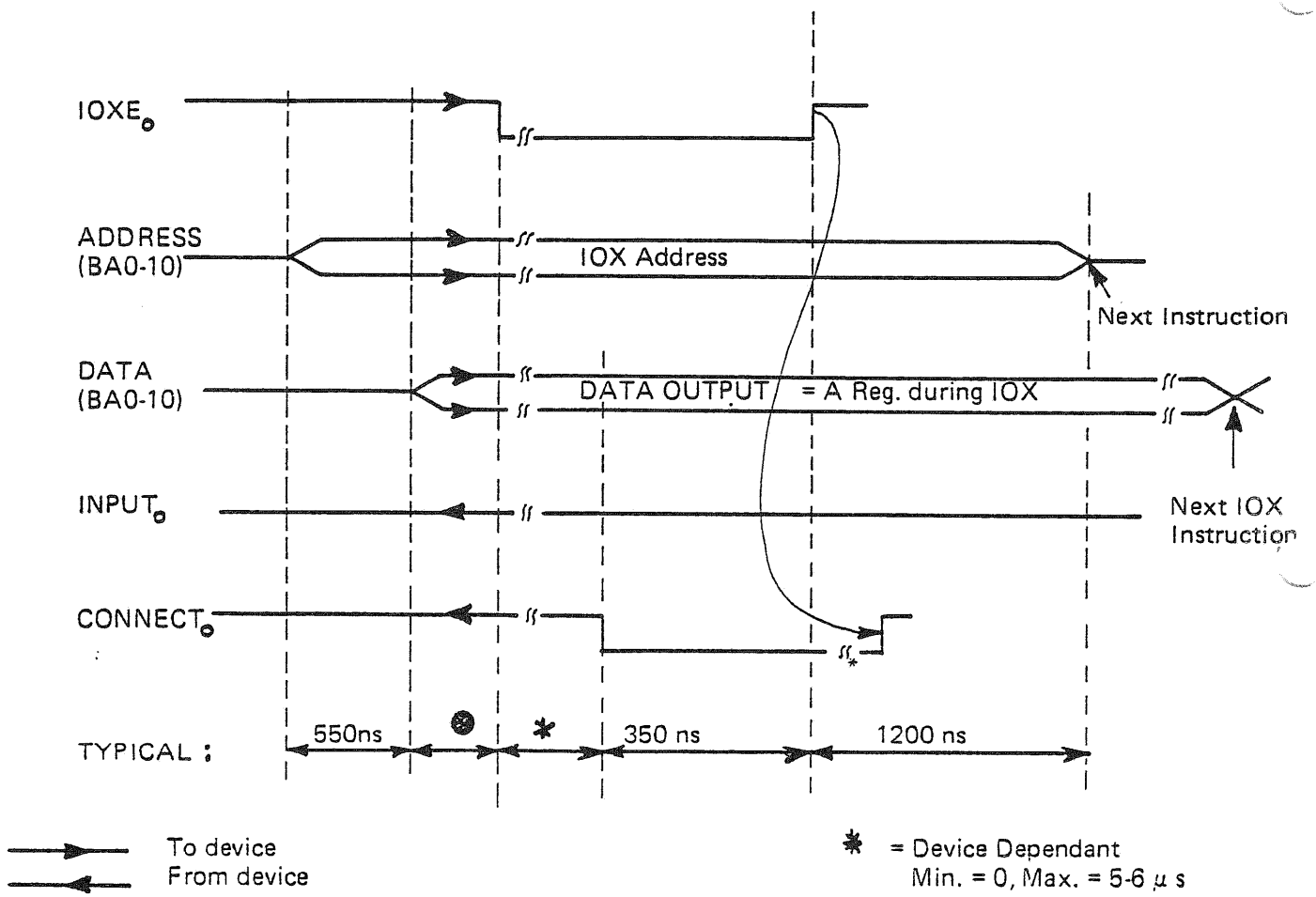


Figure 2.2: NORD-10/S COMMUNICATION WITH PIO INPUT INTERFACE

PROGRAMMED OUTPUT TO DEVICE



PROGRAMMED INPUT FROM DEVICE

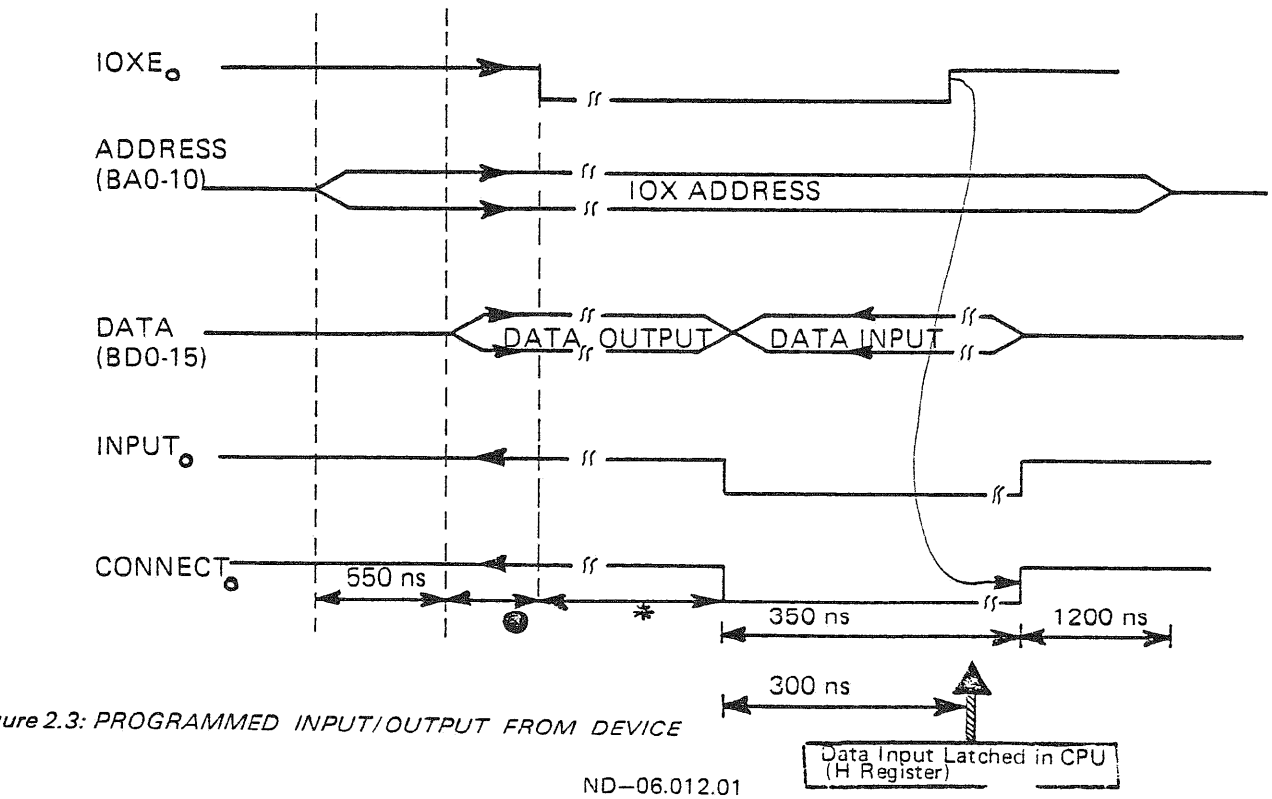


Figure 2.3: PROGRAMMED INPUT/OUTPUT FROM DEVICE

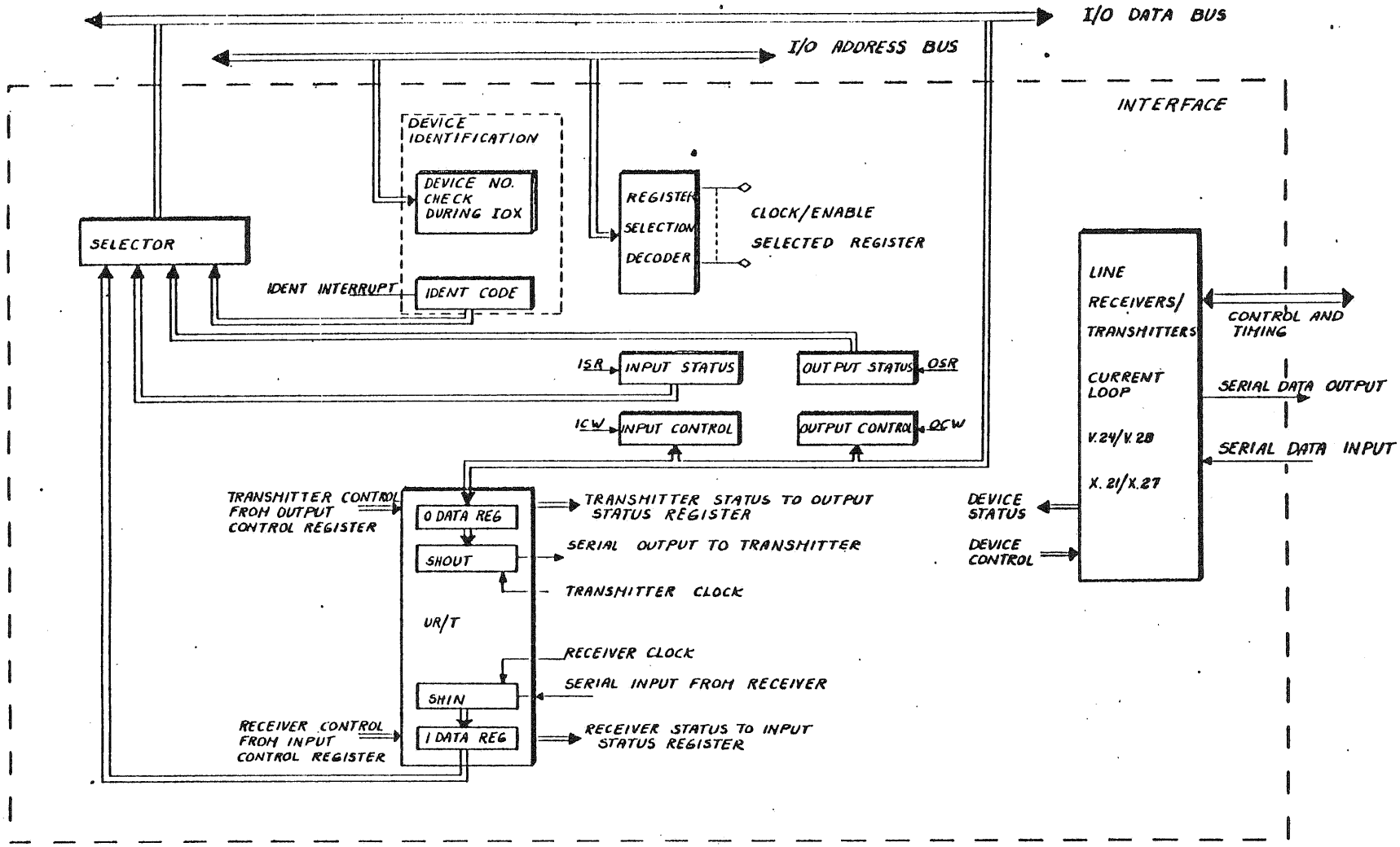


Figure 2.4: SERIAL TO PARALLEL/PARALLEL TO SERIAL PRINCIPLES

ND-06.012.01

UR/T - UNIVERSAL RECEIVER/TRANSMITTER 40 PINS LSI CHIP

- ASYNCHRONOUS INTERFACES: UART - UNIVERSAL ASYNCH. REC. TRANSM.
- SYNCHRONOUS INTERFACES: USRT - UNIVERSAL SYNCH. REC. TRANSM.
- HDLC INTERFACE: MPCC - MULTI PROTOCOL COMM. CONTROLLER

Rettet	Dato	Sign.
SERIAL TO PARALLEL PARALLEL TO SERIAL INTERFACE PRINCIPLES	Målestokk	Tegn. JP 5.5.78
		Kontr. ERO
		Appr.
A/S NORSK DATA-ELEKTRONIKK		

2.2 *IOX INSTRUCTION EXECUTION CPU*

General:

The microprogrammed NORD-10 CPU executes an IOX-instruction by fetching, clocking and decoding three micro-instructions located in the 32 bits wide Read Only Memory (ROM). In the following some remarks will be given to figure 2.5 IOX TIMING. Refer also to figure 2.6 for the CPU data and address flow.

Remark 1:

The IOX instruction is clocked into the Instruction-Register by a positive edge of the CIKL-signal, derived from the memory data ready signal MDRY. The device-address (IRO-10) is now available on the address-bus. The IREN signal is always active except during DMA. Refer to TRANSCEIVER ADDRESS module 1119.

After 200-220ns including entry-point generation, and ROM-access time, the content of ROM address 172 is clocked into the 32 bits Micro-Instruction Register (MIR) given by the following mnemonics:

172/IOX, LOGM ADIR A,A BIO D, IO (or in words):

Select the A-register through the A-operated-selector and enable it out on the IB bus. The destination is the I/O bus.

The signal TRIO is decoded from the MIR-bits and since the IOX instruction is a privileged instruction, only allowed to be executed from memory pages belonging to ring 2 or 3, the signal is checked against the Paging-Control Register bits on the Interrupt Control 1058 module. This checking takes 100ns. On the TRANSCEIVER CONTROL module 1127 the signal TRIO and TRR (decoded from MIR when A-reg-output operation) are ANDed together generating the TRRIO signal that in turn set the IOCYC flip-flop (Input/Output cycle in progress).

The RIB signal enables the IB-bus out on the D-bus (TRANSCEIVER DATA module 1125). The IOCYC flip-flop set generates a memory data-ready-signal (MDRY). This in turn clocks the second microinstruction into MIR, entering.

Remark 2:

ROM address 173:

```
LOGM A,IO BIO        % I/O-BUS→H-REGISTER
```

The TRRIO signal disappears and the D-bus is clocked into the Q latch (Q0-Q15). The IB→D bus signal (RIB) and MDRY is removed. The A-register is now available on the Main I/O Bus M0-15.The TRAIO signal decoded from the bits now in MIR generates the:

— IOXE signal; the Master Data and Address-Enabling signal

— RM signal; Enabling the M-bus out on the D-bus

— EIB signal; Enabling the D-bus out on the IB-bus

The CONNECT signal will be returned from the device interface recognizing the address together with the INPUT signal. The returned CONNECT-signal is delayed (DCON), ensuring stable data on the M-bus.

EM signal generation:

At DCON time the EM signal is generated depending on the state of the returned INPUT-signal.

INPUT TRUE (EM not TRUE):

—The Q latch is disabled from the M-bus. Data to IB is taken from the MAIN I/O data-bus.

INPUT NOT TRUE (EM TRUE):

—The Q latch is enabled onto the M-bus and fed back to the IB bus.

The DCON signal generates a memory-data ready signal (MDRY) and the IB-bus is clocked into the H-register. If no CONNECT signal is returned from the addressed interface within 5-6 μs, a TIMEOUT signal is generated.

The TIMEOUT signal does:

— 1. Generate a MDRY signal for hang-up prevention.

— 2. Generate a internal-interrupt to level 14 (IOERR) if Interrupt-system is turned on.

The MDRY signal in turn clocks the third microinstruction into MIR entering.

Remark 3:

MIR now contains:

LOGM CFC ADIR A,H D,A % H-REG→A-REG NEXT-INSTRUCTION FETCH.

The TRAIO; IOXE; EIB and the RM signals disappear and as a response to removed IOXE, the CONNECT and INPUT signal will be dropped by the device-interface.

A removed CONNECT signal will reset the IOCYC flip-flop, indicating the I/O BUS is ready for new activity (DMA transfer or a new IOX).

During the activities mentioned, the H-register is selected as A-operand direct through the most significant arithmetic and enabled onto the most significant SUM-bus. In parallel with the H-register through the arithmetic, the next instruction is fetched from main memory. The next instruction is clocked into IR and the SUM-bus is clocked into the A-register, ending the story of the IOX instruction with this GENERAL REMARK:

—If an OUTPUT-operation, the content of the A-register is written back to itself.

—If an INPUT-operation, the data enabled out on the I/O data-bus is written into the A-register.

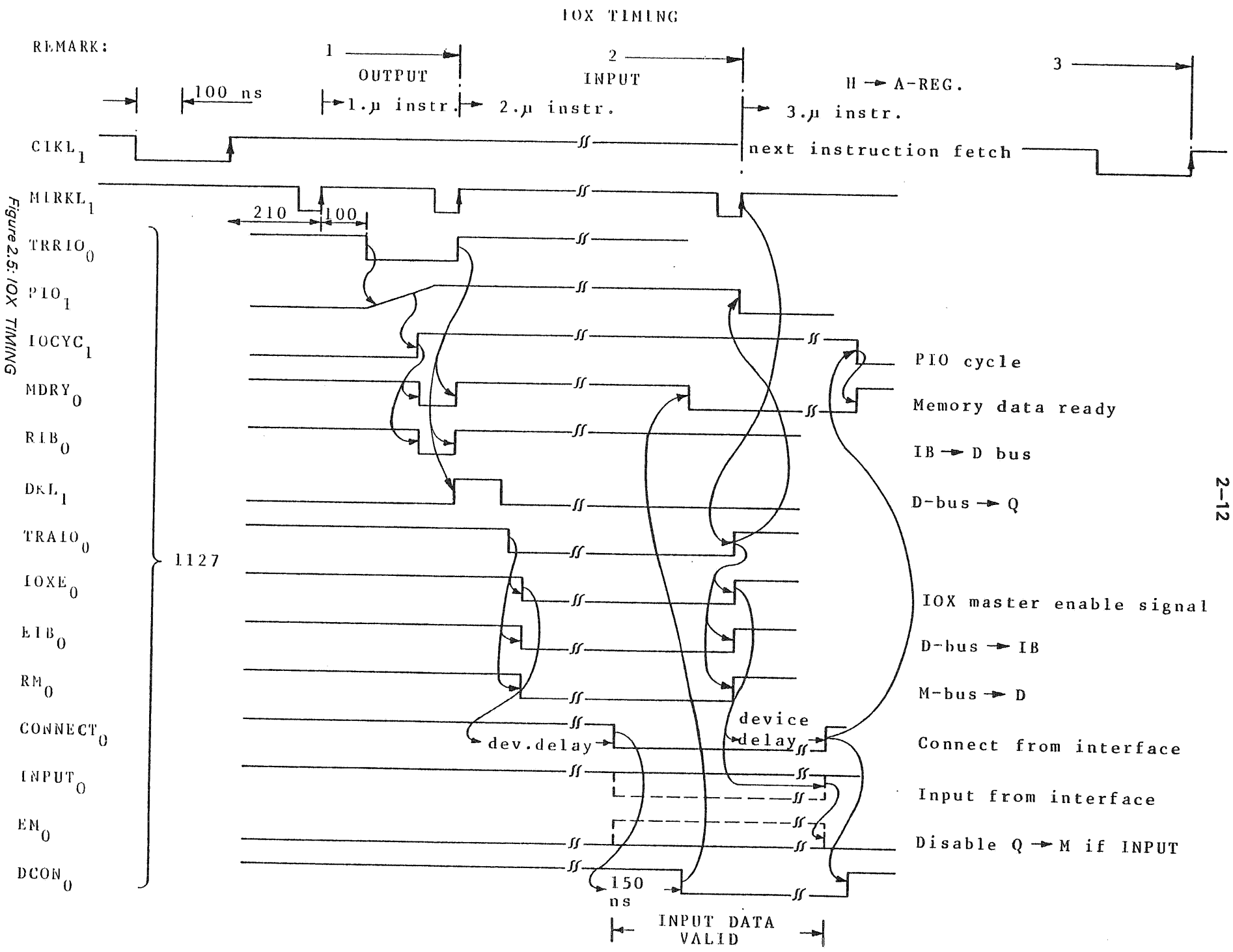


Figure 2.5: IOX TIMING

ND-06.012.01

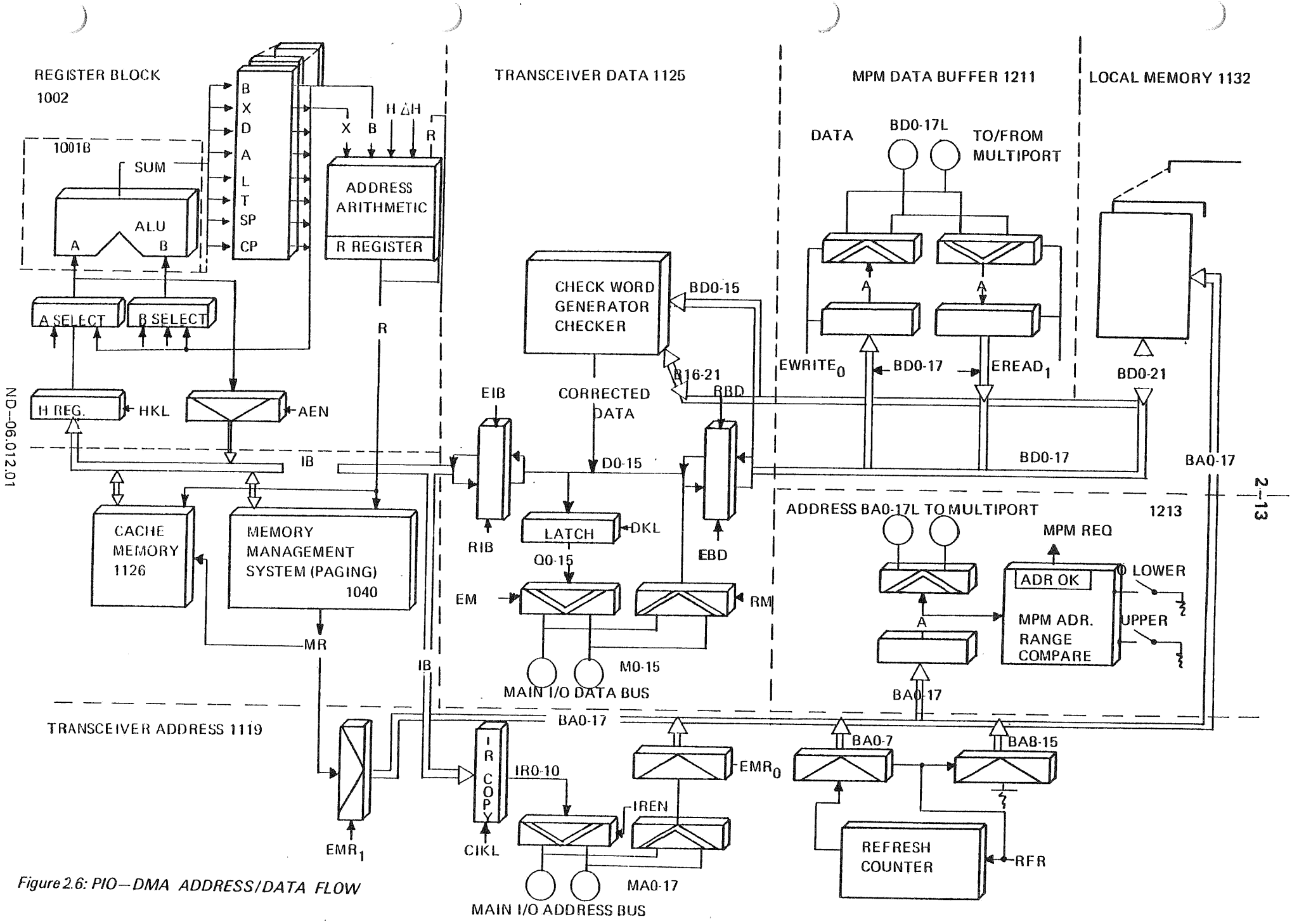
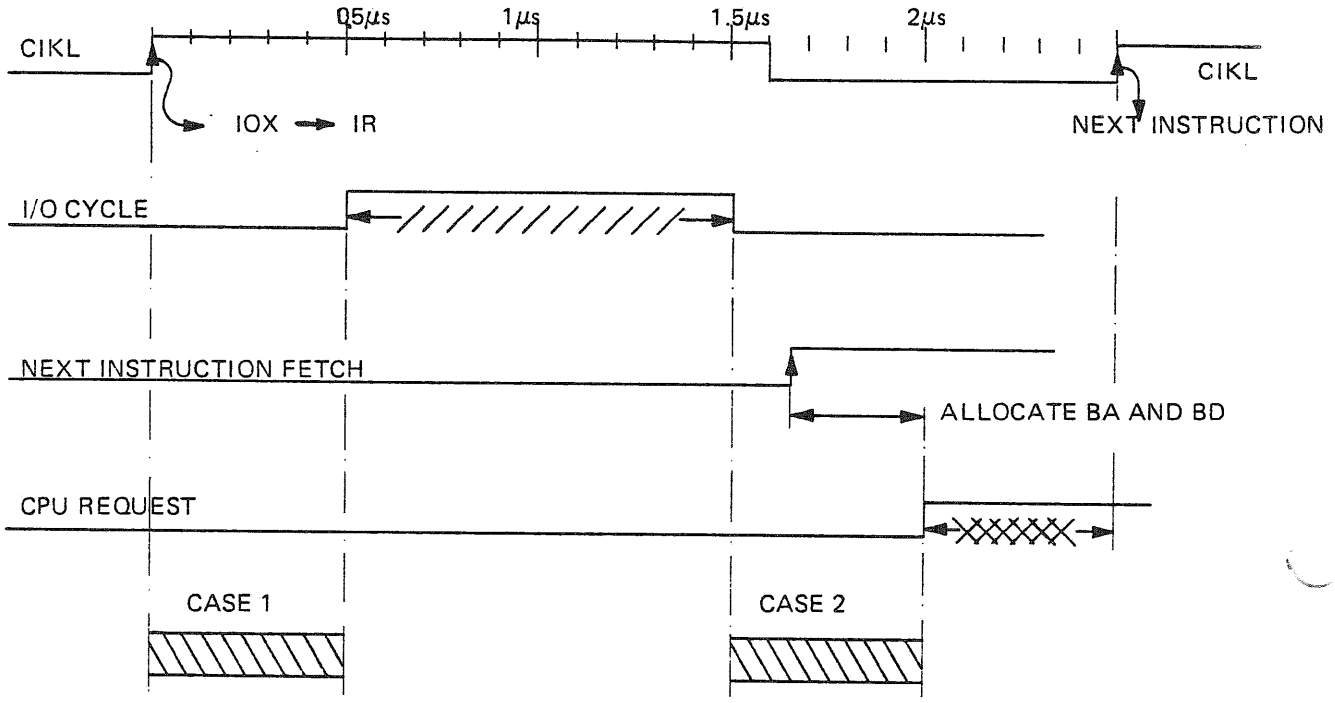


Figure 2.6: PIO—DMA ADDRESS/DATA FLOW

IOX EXECUTION AND BUS USAGE



//////// The Main and Local IO bus is used by the IOX instruction. The CPU data bus IB is also allocated for the IOX instruction.

Duration: from 1-5 µs, dependent on device response.

XXXXXXXX The memory address bus BA and data bus BD together with the IB bus is allocated the CPU.

Duration: this time depends on the memory response time .

Typical:

0.5 µs for local memory
1.0 µs for multiport memory

\\\\\\\\\ In this period the I/O Bus may be allocated a DMA-transfer to the local memory or multiport memory via the CPU port.

CASE 1: The IOCYCLE is started when the DMA-transfer has finished.

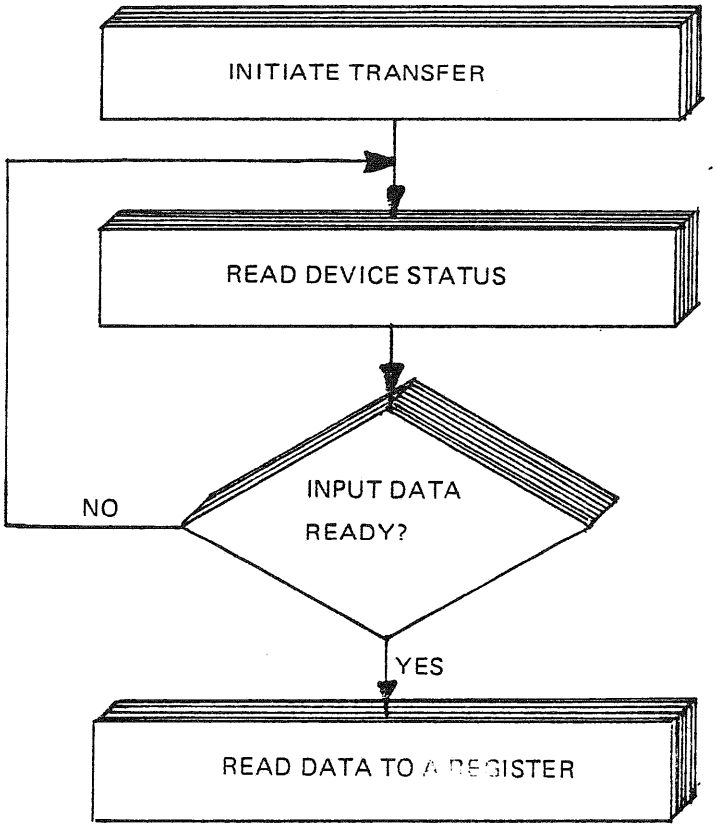
CASE 2: The CPU Request must wait until the DMA-transfer has finished.

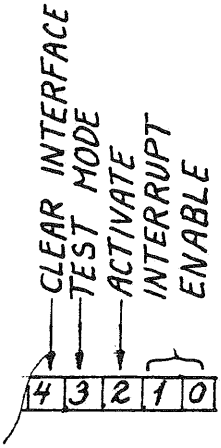
Figure 2.7: IOX EXECUTION AND BUS USAGE

2.3 *PROGRAMMING A PIO INTERFACE*

INPUT

The flow diagram below shows the communication between the CPU and the interface for reading one word or byte of data.





CW

The transfer is initiated by setting the CONTROL-WORD REGISTER informing of:

- —Mode of operation
- —Interrupt enabling
- —Device activation

LDA CW
IOX LCW

The presence of input-data is checked by reading the STATUS-register. Bit 3 in the interface status register is set to a one when parallel data is clocked or serial data is assembled in the DATA-register.

```
LOOP, IOX RSTAT
        BSKP ONE 30 DA
        JMP LOOP
```

The program will loop until bit 3 in the STATUS-REGISTER is set. The data can now be transferred to the A-register.

The advantage of interrupt-programming is clearly stated by this looping waiting for the DATA-READY.

WITHOUT INTERRUPT:

The CPU will do nothing but monitor bit 3 in the status register.

WITH INTERRUPT:

With the interrupt system in the CPU turned on, and the interface enabled for interrupt, the interface will tell the CPU when the DATA is READY by means of an interrupt signal. This enables the CPU to do other tasks while the data-transfer takes place.

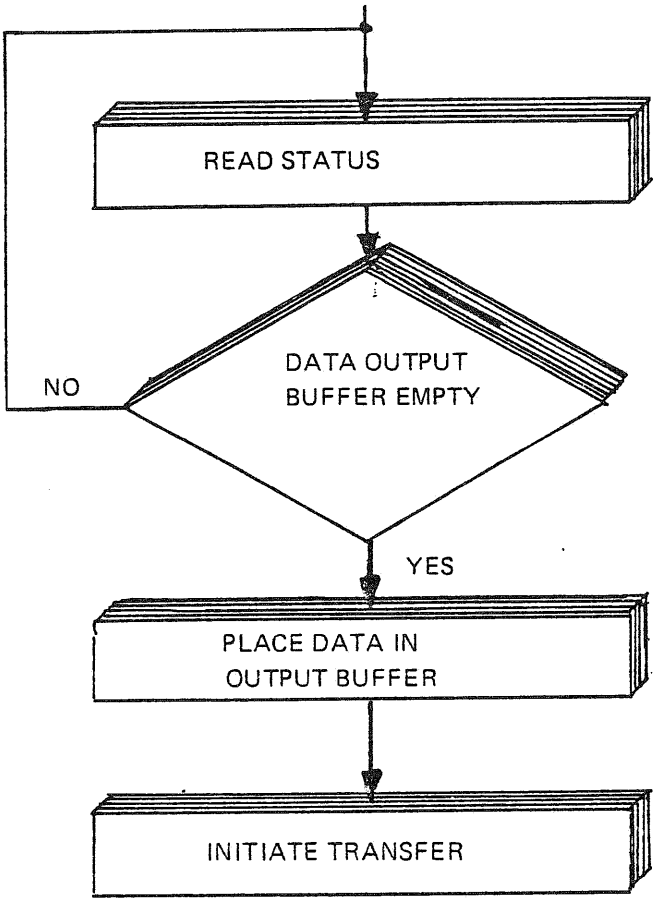
Example:

With the interrupt system turned on the CPU can execute about 1500-2200 instructions between two DATA-READY (sprocket) pulses when reading data from a TAPE-READER (330 character/sec).

At DATA-READY time the data is transferred to the A-register by means of an IOX read-data register instruction.

The data must then be stored away before the next transfer is initialized.

OUTPUT:



The interface STATUS-REGISTER is read, and bit 3 is checked for a 1. If a 1, this implies that the previous data transfer was finished and new data can be placed in the output data buffer. If NOT, loop.

IOX RSTAT
BSK? ONE 30 DA
JM: *-2

BIT 3=1

Transfer A-register to output-buffer:

IOX WDATA

Transfer A-register to control-word register:

IOX LCW

With bit 2 set to a one:

This will initiate the move of data from the buffer-register in the interface to the physical device.

2.3.1 *FORMAT OF STATUS AND CONTROL WORD*

The format of status and control word may be assigned by the designer of each device controller. The following standard is used by ND for its own device control cards (when applicable) and is recommended for customer use.

STATUS WORD

Bit 0	Ready for transfer, interrupt enabled
Bit 1	Error interrupt enabled
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors
Bit 5	Error indicator
Bit 6	Error indicator
Bit 7	Error indicator
Bit 8	Error indicator
Bit 9	Selected unit
Bit 10	Selected unit
Bit 11	Operational mode of device
Bit 12	Operational mode of device
Bit 13	Operational mode of device
Bit 14	Operational mode of device
Bit 15	Operational mode of device

CONTROL WORD

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Enable interrupt on errors
Bit 2	Activate device
Bit 3	Test mode
Bit 4	Device clear
Bit 5	Address bit 16
Bit 6	Address bit 17
Bit 7	Not assigned
Bit 8	Not assigned
Bit 9	Unit
Bit 10	Unit
Bit 11	Device operation
Bit 12	Device operation
Bit 13	Device operation
Bit 14	Device operation
Bit 15	Device operation

3 PROGRAMMED INPUT/OUTPUT LOCAL I/O BUS SIGNALS

The following signals on the local I/O Bus are relevant for programmed input/output:

	Name:
DATA	BD xx
ADDRESS	BA xx
IOXE	BIOXE
CONNECT	BCONNECT
INPUT	BINPUT
MASTER CLEAR	BMC

16 DATA Source: Device or CPU

16 tristate lines carrying the data information from the CPU or from the device depending upon the control signal INPUT.

11 ADDRESS Source: CPU

Bit 0-9: Gives the value of the 10 least significant bits of the CPU instruction register, i.e., the device register address during an IOX-instruction.

Bit 10: Instruction register bit 10.
IR10 = 0 ND standard interfaces
IR10 = 1 Customer produced interfaces.

1 IOXE Source: CPU

IOX instruction master enable and timing signals. On the BRANCH CONTROL module this signal is input to circuits generating either a local IOXE (BIOXE) or an external IOXE (EIOXE) signal. Whether to generate BIOXE or EIOXE is given by IR bit 10 and a strap on the BRANCH CONTROL module.

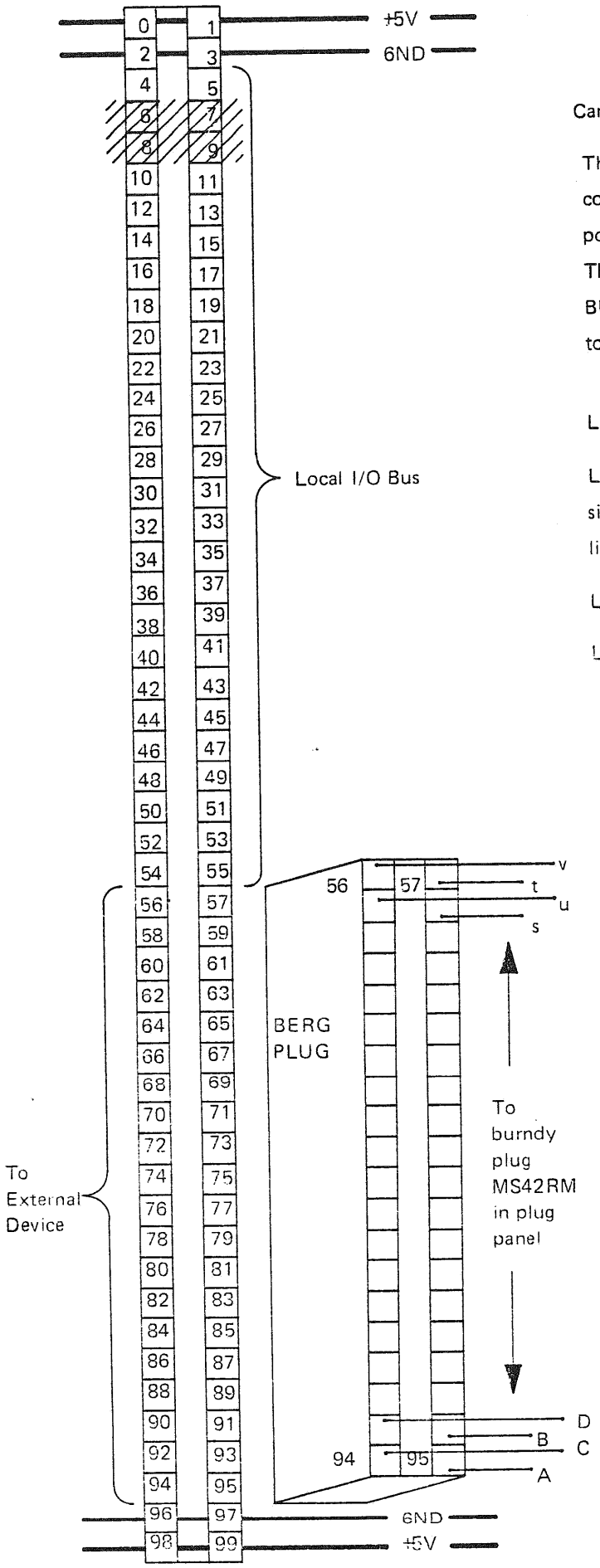
1 BIOXE Source: BRANCHER

If strap closed: Local IOXE signal for IR10 = 0): Address <2000
If strap open: Local IOXE signal for IR10 = 1): Address >2000

1 EIOXE* Source: BRANCHER

External IOXE signal supplied to the customer via the bus driver/receiver modules.
*This signal is not in the local I/O bus.

1 CONNECT Source: Device	A device answer on the IOXE signal has been received and that the device has: — Decoded the ADDRESS bits 0-9 and recognized one of its device register addresses. — If INPUT: The input DATA is enabled out on the BD data-bus —If OUTPUT: The DATA on the BD-bus equal the A-register is taken care of by the device CONNECT has to be returned within a specified time (max.5-6μs) otherwise the CPU will generate an internal interrupt on level 14 (IOX error).
1 INPUT Source: Device	Defines the direction of the data lines. INPUT true; data transferred from device to CPU A-register. INPUT false; data transferred from CPU A-register to device.
1 MASTER CLEAR Source: CPU	Used to clear the logic in the device controllers.



Card Module:

The interface module is fit into a 100 terminal connector where 4 of the terminals are used for power (+5V) and 4 terminals for ground (GND). The terminals 4-55 are assigned for the local I/O BUS, while terminal 56-95 are used for connection to the external device via the plug-panel.

Local I/O Bus Signal Levels:

Local I/O Bus signals are TRI-STATE TTL for all signals except interrupt lines and DMA request line, which are open collector TTL.

Logical "1" signal $0 \leq S \leq 0{,}4V$

Logical "0" signal $2{,}4 \leq S \leq 5V$

These terminals do not have a 1-1 connection to the next I/O position (used for IDENT and GRANT)

Figure 3.1: I/O SLOT/PLUG LAYOUT

4 I/O INTERRUPT-SYSTEM

In this chapter some general remarks regarding the NORD-10/S interrupt system will be given together with information about the IDENT instruction.

4.1 *NORD-10/S INTERRUPT SYSTEM GENERAL DESCRIPTION*

The interrupt system consists of 16 program levels in hardware, each program level with its own complete set of general registers and status indicator. The program levels are numbered from 0 to 15 with increasing priority; program level 15 has the highest priority, program level 0 has the lowest.

The program levels are controlled from the two 16-bit registers:

— PIE-Priority Interrupt Enable Register

— PID-Priority Interrupt Detect Register

Each program level is controlled by the corresponding bits in these registers. The PIE register is program controlled, set from the A-register, and the PID register is controlled by both program and external asynchronous interrupt. At any time, the highest program level, which has its corresponding bits set in both PIE and PID, is running. This level is called PL, current program level. Refer also to figure 4.1.

A change from a lower to a higher program level occurs when a bit in the PID register with higher priority than the running one is set. (The corresponding PIE bit must also be a one). This setting of the PID-register can take place in two ways:

1. Set by program; Programmed Interrupt
2. Set by the I/O system (PID bit 15, 13, 12, 11 and 10); I/O interrupt

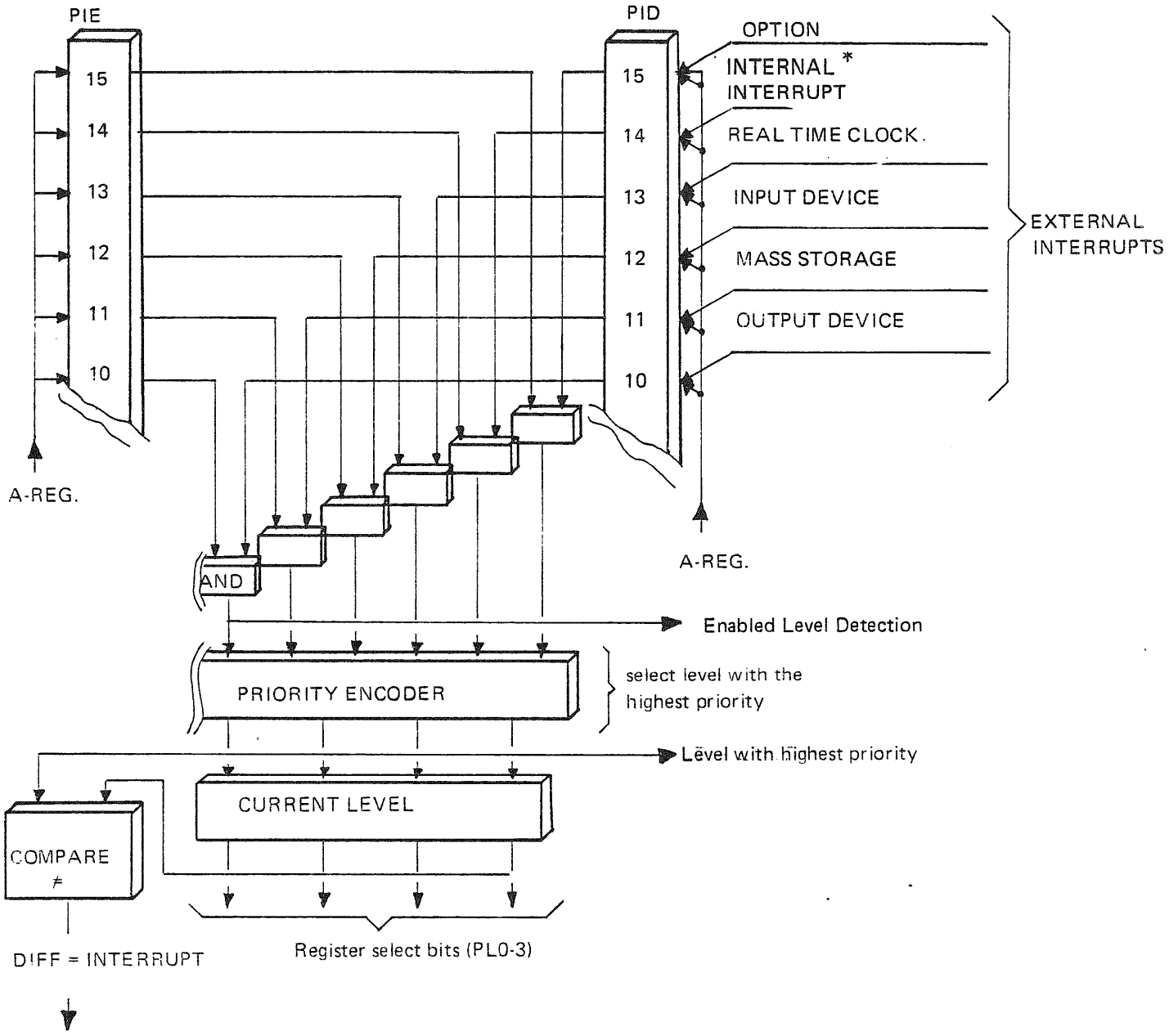
A change from a higher program level to a lower takes place when the program on the higher program level gives up its priority. This done by executing a WAIT instruction on the current level.

At CHANGE-LEVEL time, this takes place in hardware:

1) The current program-level address is saved in the saved program counter, SP register. CP→$SP_{current\ level}$.

2) The current-level indicator is set with the new level (4 bits code PL0-3). Selecting the register block for the new level.

3) The SP for the new level is transferred to Current Program Counter CP. $SP_{new\ level}$→CP.



* Internal interrupt LEVEL 14 NO CONNECT error, IOX—timeout is one source.

Figure 4.1: NORD-10/S INTERRUPT SYSTEM

4.2 *I/O INTERRUPT*

External interrupts may set PID bits 15,13,12,11 and 10. Program level 15 is not used by standard NORD equipment or software but is available for users who need immediate access to the CPU.

LEVEL:

13: Real Time Clock interrupt (Interrupt every 20ms.)

12: Input devices

11: Mass-storage or DMA devices

10: Output devices

An interrupt on level 12-10 may occur for two reasons:

1. Data Ready interrupt
   or
2. Error interrupt

A Data Ready interrupt indicates that for an input device, the data is ready to be transferred to the A-register. For an output device, the output-buffer is empty and new data may be transferred from the A-register to the buffer.

A Data Ready interrupt from a DMA-device indicates that the data-transfer is completed.

An Error Interrupt will occur if the data transfer was unsuccessful.

4.3 *INTERRUPT IDENTIFICATION*

For program levels 10,11,12 and 13 it is required to identify the I/O interrupt when it occurs, since several sources may be connected to the same level. This identification process is available through the instruction:

IDENT <program level>

The IDENT instruction is used to identify and service the actual interface that generated the interrupt. Actually there are four IDENT instructions, one to identify and service I/O interrupts on each of the four levels 10,11,12 and 13.

The four instructions are:

IDENT	PL10	Identify Input/Output interrupt on level 10	Code:143604
IDENT	PL11	Identify Input/Output interrupt on level 11	Code:143611
IDENT	PL12	Identify Input/Output interrupt on level 12	Code:143622
IDENT	PL13	Identify Input/Output interrupt on level 13	Code:143643

The result of the IDENT instruction is a unique identification code returned from the interrupting interface to the A-register. The 9 bits code is given in A-reg bits 0-8, with bits 9-15 all zeros.

If the IDENT instruction is executed, but there is no device to serve, the A-register is unchanged. An IOX error interrupt to level 14 (TIMEOUT) will occur if enabled.

If several devices on the same program level have simultaneous interrupts, the priority is determined by which Input/Output slot the device is plugged into. The interrupt line to the corresponding PID bit will remain active until all devices have been serviced. When an interface responds to an IDENT, the INTERRUPT-ENABLE flip-flop is turned off, and the interrupt-signal is dropped. The INTERRUPT-ENABLE flip-flop must then be set by software before the next interrupt can be handled.

For program level 15, however there is no IDENT instruction, since there should be only one source for this interrupt.

4.4 *IDENT-INSTRUCTION*

The four IDENT-instructions have the following format:

INSTRUCTION:	*CODE:*	*BIT 0-5 IN CODE:*					
		5	4	3	2	1	0
IDENT PL10	143604	0	0	0	1	0	0
IDENT PL11	143611	0	0	1	0	0	1
IDENT PL12	143622	0	1	0	0	1	0
IDENT PL13	143643	1	0	0	0	1	1
		Mask-Code			Count-Code		

The codes for the different program-levels in the IDENT-instruction are chosen for the following reason:

To make it easy for the hardware to verify the correspondence between the interrupt-level and the IDENT instruction.

For example:

Executing an IDENT Program Level 12, only the interface connected to Level 12 should return the IDENT-CODE.

4.5 *IDENT-INSTRUCTION-EXECUTION SEQUENCE*

In the local I/O bus, five terminals are set off for carrying the interrupt-signals.

Signal:	*Terminal:*	*Means:*
BINT 10	27	Interrupt to level 10
BINT 11	31	Interrupt to level 11
BINT 12	35	Interrupt to level 12
BINT 13	39	Interrupt to level 13
BINT 15	43	Interrupt to level 15

On a two-way interface module the INPUT part will be connected to terminal 35 (BINT 12) and the OUTPUT-part will be connected to terminal 27 (BINT 10). The rest of the interface-modules will only be connected to one interrupt-terminal.

The BINT 10-13 are open-collector lines ORing all interrupts in the local I/O BUS.

The BINT 10-13 are connected to the PID bits in the CPU via the BRANCH CONTROL (1101) in the I/O-rack and TRANSCEIVER-CONTROL (1127) module in the CPU-rack. The interrupt signal will force the CPU to change level if CPU was executing on a level with lower priority. The driver on the relevant level will execute an IDENT PL instruction. The ROM-memory entry-point for the IDENT equals 217, but this location contains only a microprogram jump to address 172 equal the IOX instruction entry point. The timing for executing an IDENT instruction and an IOX instruction will be simular apart from the following:

— On the address-bus BA, there is no device address, but code bits for checking the interrupt level and IDENT instruction.

— During the second microinstruction no IOXE signal but an IDENT-signal is generated on the TRANSCEIVER CONTROL 1127 module. Instruction register bit 13 = 1 during an IOX instruction and = 0 during an IDENT-instruction.

Refer to figure 4.2.

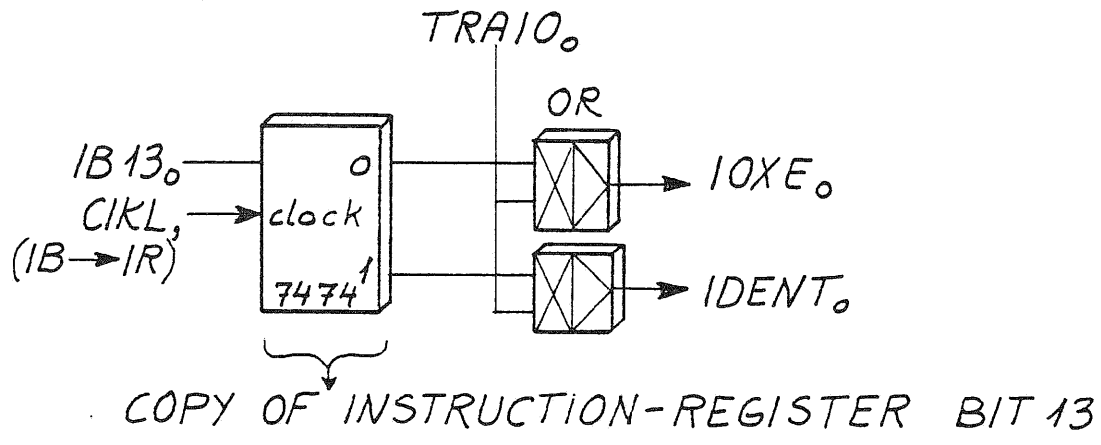


Figure 4.2: IOXE/IDENT SIGNAL GENERATION

The IDENT signal is received in the BRANCH-CONTROL 1101 module in the I/O-rack. In this module the signal is checked against the interrupt-lines BINT 10-13. If there was an external interrupt from the next I/O rack, an OUTIDENT signal is sent to the next rack. Otherwise a LOCAL IDENT signal (BIDENT) is generated.

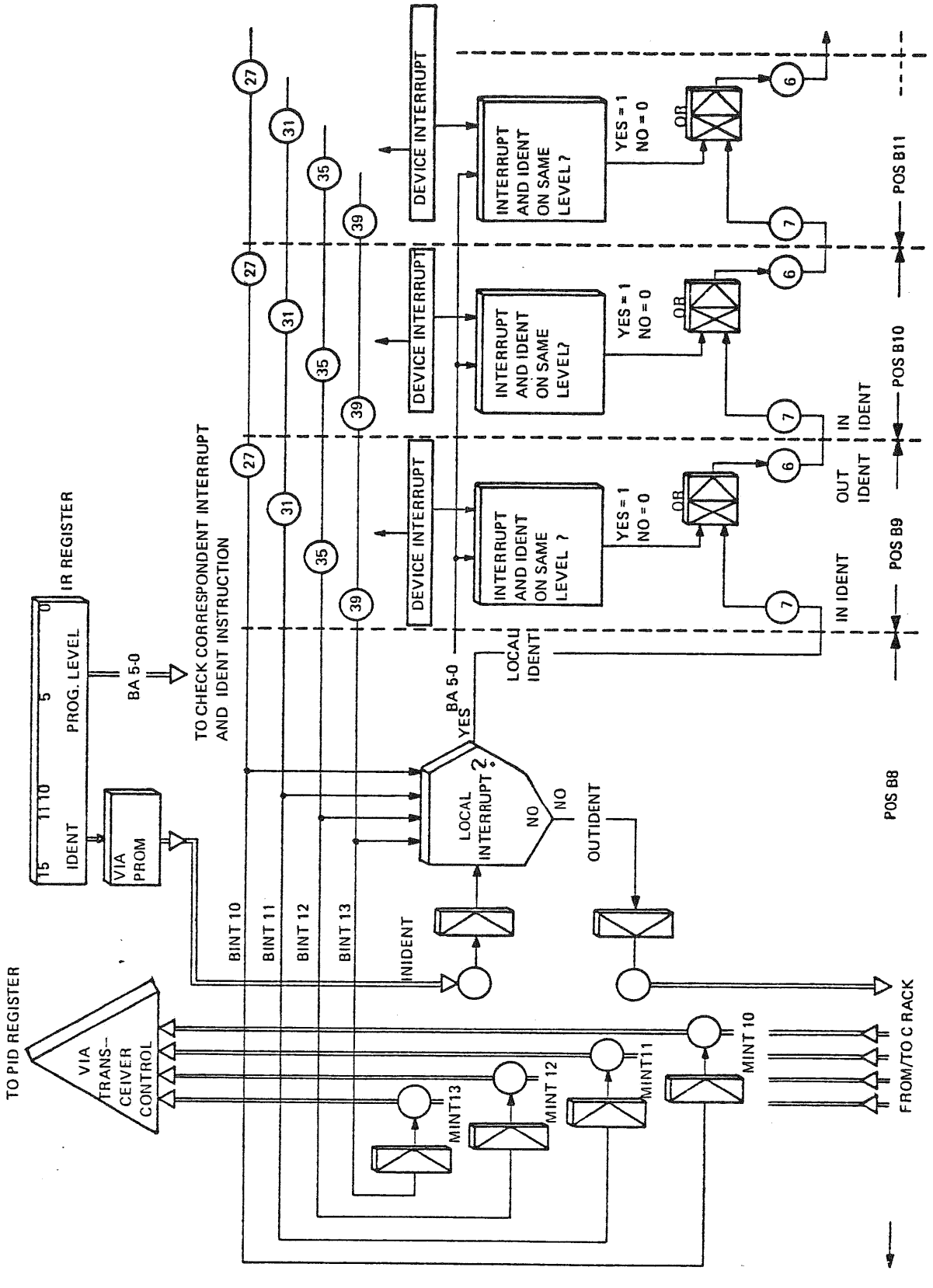


Figure 4.3: IDENT OVERVIEW

The first device receiving the BIDENT signal, called INIDENT on the module, is the first device in the interrupt priority chain. If this device gave no interrupt or the INIDENT signal was for a different level, the device will send the INIDENT signal as the OUTIDENT from this device. The next device in the priority chain will now receive this signal as its INIDENT. This daisy chaining will continue until the device that gave the interrupt recognizes the INIDENT and finds that the code for the interrupt level ADDRESS BITS 0-5 corresponds to the level for the specific device. This device will *not* transmit an OUTIDENT signal. The device will instead return a CONNECT and an INPUT signal together with the IDENT CODE. The IDENT CODE is enabled out on the DATA-BUS (BD).

IDENT DETAILS ON ONE CARD

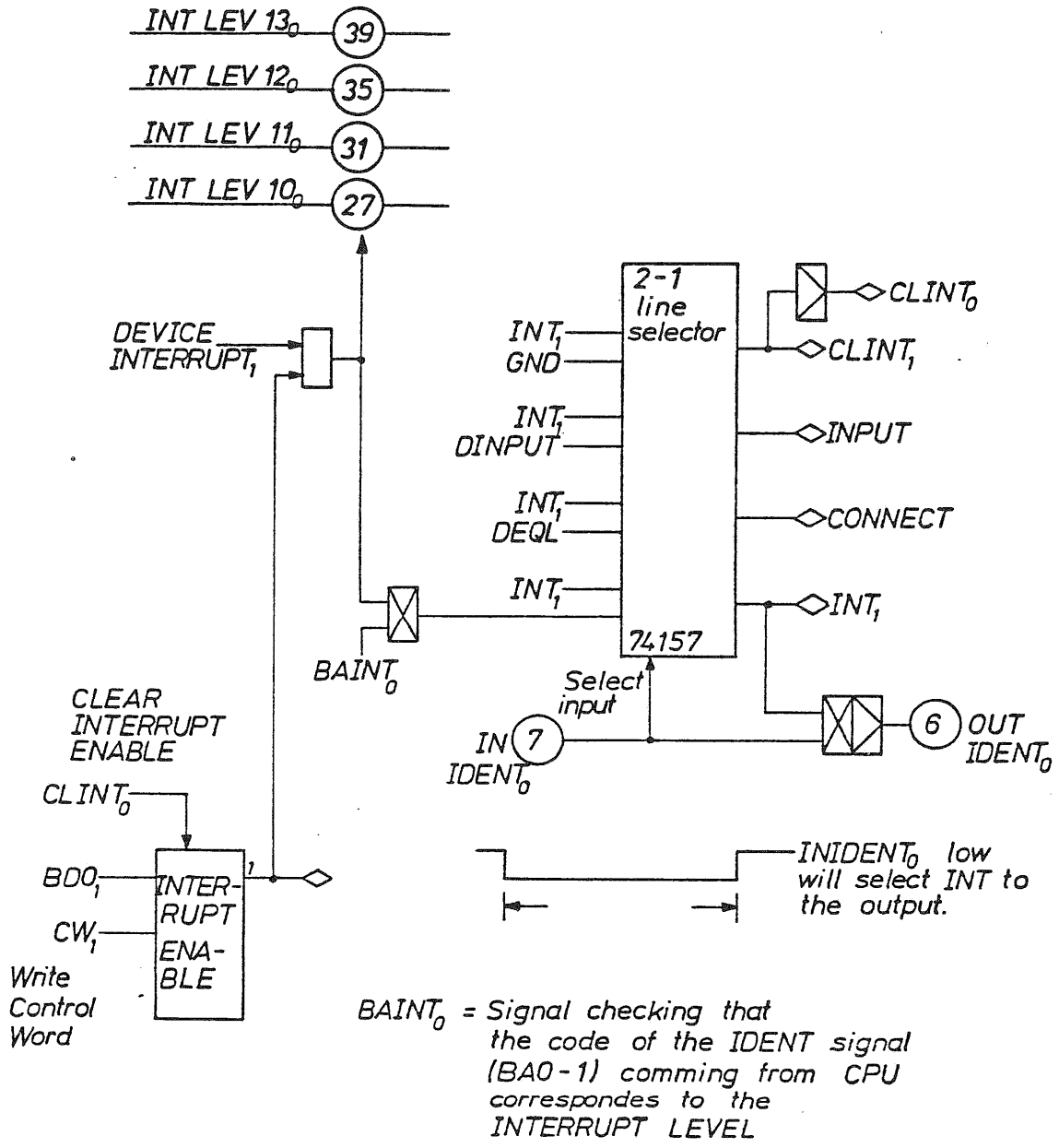


Figure 4.4: IDENT DETAILS ON ONE CARD Tegn. 6.7.76.PK/BW

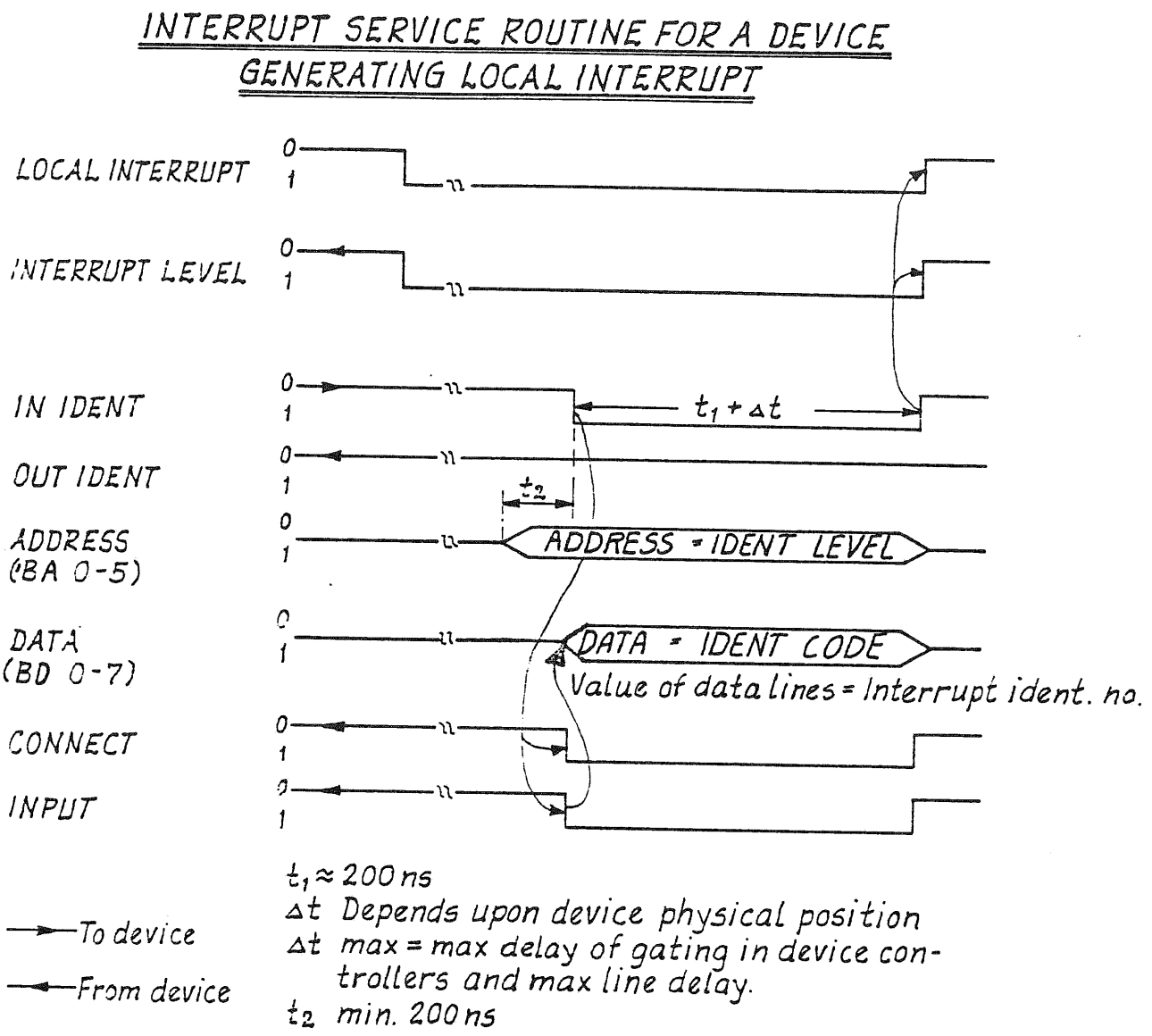


Figure 4.5: INTERRUPT SERVICE ROUTINE FOR A DEVICE GENERATING LOCAL INTERRUPT

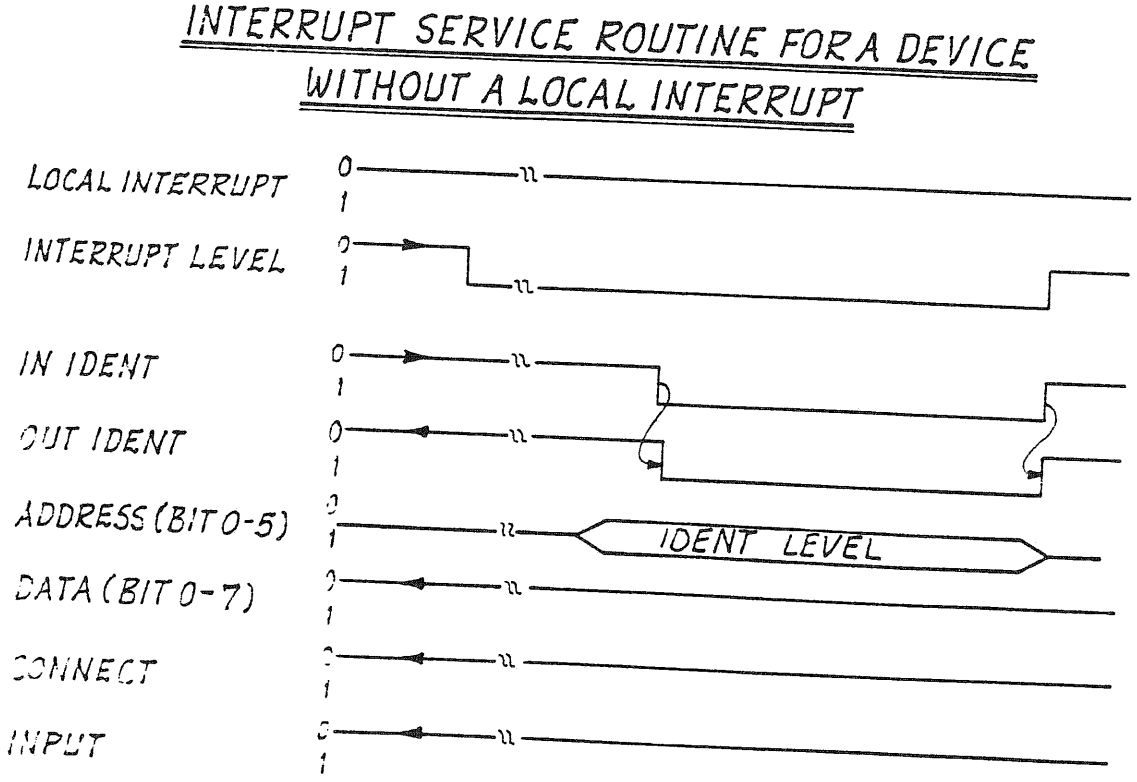


Figure 4.6: INTERRUPT SERVICE ROUTINE FOR A DEVICE WITHOUT A LOCAL INTERRUPT

4.6 *INTERRUPT IDENTIFICATION SIGNALS*

Bus Signals

The following signals on the I/O Bus are relevant during an interrupt/ident sequence:

	Name:
DATA	BD xx
ADDRESS	BA xx
INTERRUPT	BINT 10,11,12,13 and 15
INIDENT	INIDENT
OUTIDENT	OUTIDENT
CONNECT	BCONNECT
INPUT	BINPUT
MASTER CLEAR	BMC

9 DATA
Source:
Interface

Bit 0-7: The value of these lines is equal to the specific INTERRUPT IDENTIFICATION NO. for the device. Each physical device is given a unique interrupt identification number. The INTERRUPT IDENTIFICATION NO. is normally given by switches or straps on the interface module.

Bit 8: For customer-equipment with device addresses >2000 this bit should always be a 1 in the returned IDENT CODE. This for separating the customer IDENT CODE $>400_8$ from the ND IDENT CODE $<400_8$.

The addition of this bit is switch-controlled on the CONTROL-DRIVER module 1073.

6 ADDRESS
Source:
CPU

Bits 0-5: Give a coded value for the external interrupt level where the program is seeking to identify an interrupt.

5 INTERRUPT
Source:
Interface

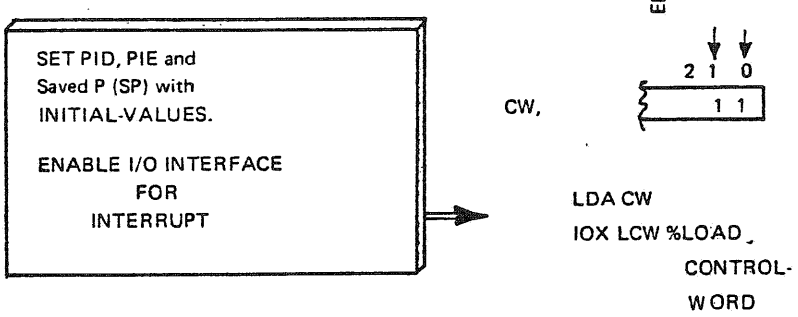
One line for each external interrupt level (10,11,12,13 and 15). When the device wants the CPU attention one of these lines is grounded - set true. The level has to remain true until the device has been serviced by the IDENT instruction for the specific level. These signals are open collector signals in the local I/O BUS.

1 INIDENT Source: CPU and interface	This signal is generated at the CPU as a decoding of one of the four IDENT instructions.
1 OUTIDENT Source: Interface	A signal transmitted to the next device's INIDENT pin if the device did not generate an INTERRUPT or the interrupt code did not correspond to the interrupt level of the device.
1 CONNECT Source: Interface	A device answer on the INIDENT indicating that the device that gave the INTERRUPT has recognized the INIDENT and found the code for the interrupt level to correspond to the level of its specific interrupt.
1 INPUT Source: Interface	A line indicating that the connected device is returning its DEVICE IDENTIFICATION NO. on the DATA lines. BD.
1 MASTER CLEAR Source: CPU	Used to clear the logic in the device controllers.

4.7 *INPUT/OUTPUT INTERRUPT PROGRAMMING:*

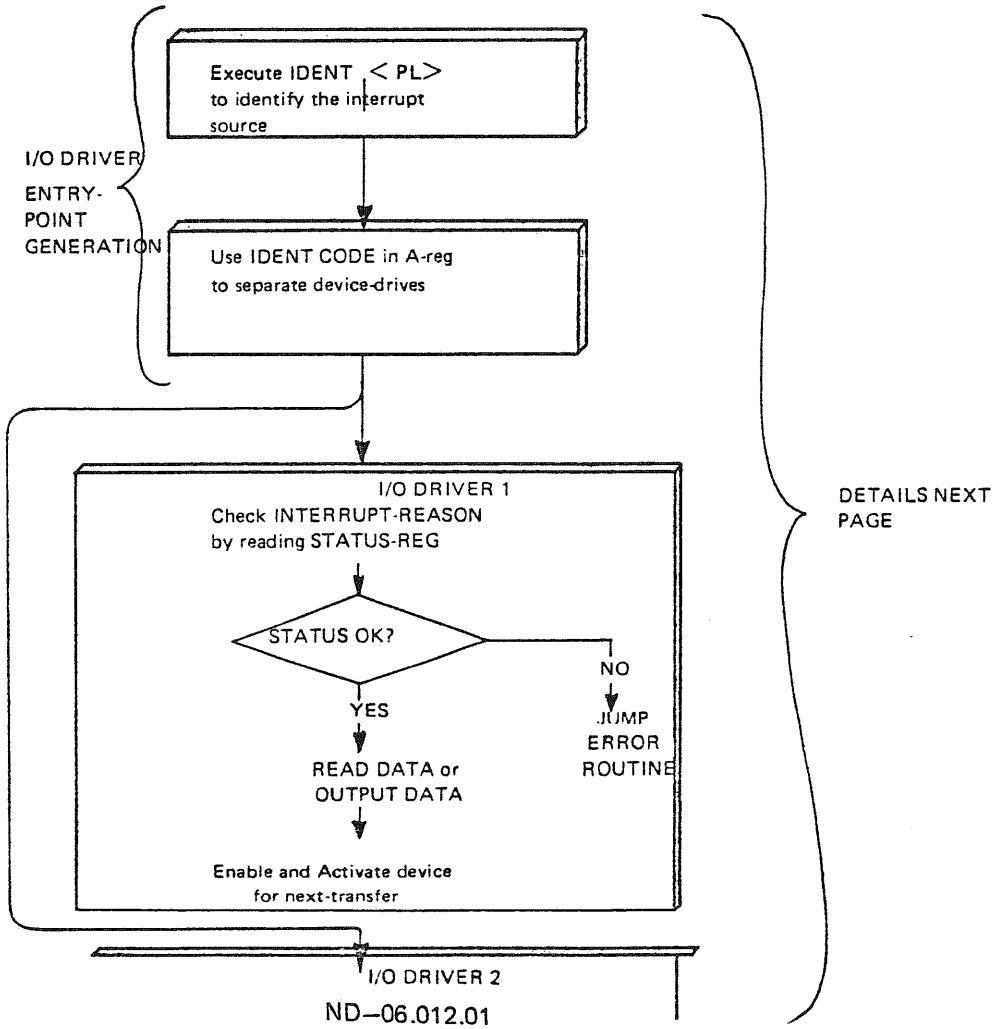
Design of an Input/Output Handler Routine

AT INIALIZATION TIME:



AT INTERRUPT TIME:

Input/Output handling routine on interrupting level



This is an example of a simple Input/Output driver system:

```
% PROGRAM ON LEVEL 12
RET,    WAIT
INT12,  SAA 0
        IDENT PL12          % GET INTERRUPT IDENTIFICATION
        RADD SA DP          % ADD NUMBER TO P REGISTER
        JMP ERROR           % IDENT 0 MEANS I/O
                            % SYSTEM ERROR
        JMP DRIVER1         % GO TO 1. DRIVER
        JMP DRIVER2
—
        JMP DRIVERN
% DRIVER FOR AN INPUT DEVICE
DRIVER1, IOX  STATUS        % READ DEVICE STATUS
        BSKP ZRO 40 DA
        JMP ERRORD          % DEVICE ERROR
        IOX RBUF            % READ DEVICE BUFFER
        STA BUFF            % SAVE DATA
        —
        —
        % ENABLE AND ACTIVATE DEVICE FOR NEXT TRANSFER
        JMP RET
```

5 BUS-RECEIVER/BRANCHER

This chapter will deal with the BUS-RECEIVER/BRANCHER and the hardware modules involved.

5.1 *GENERAL*

The 8 left-most positions in an I/O card crate are assigned for modules converting the differential-line MAIN I/O BUS to the tristate LOCAL I/O BUS. Three positions; 3,4 and 6 are set off for plug-expansion of the MAIN I/O BUS to the next I/O rack.

Module usage (Refer to Figure 5.1):

—If the I/O card crate contains only PIO interfaces, the simplest state is used.

1 module for DATA (16 bits)
1 module for ADDRESS output (11 bits) = IRO-10
1 module for CONTROL

—If a DMA interface is installed in the rack:*

1 additional module containing the Memory Address Register (CAR) is inserted in position 1.

—If a DMA transfer direct to the Multiport is desired:*

1 module is added to handle the data to/from multiport. When this module is added (Pos 8) the following will happen:

The local data-bus BD is routed direct to/from multiport memory via the module in position 8.

DMA-addresses are sent direct to multiport-memory from module in position 1.

Control-signals during a DMA-transfer (REQUEST, DATA-READY and WRITE) are disabled from the Main I/O bus and routed direct to/from multiport.

NB! To achieve this new cabling and an extra port in memory is required.

* More DMA information in Chapter 6.

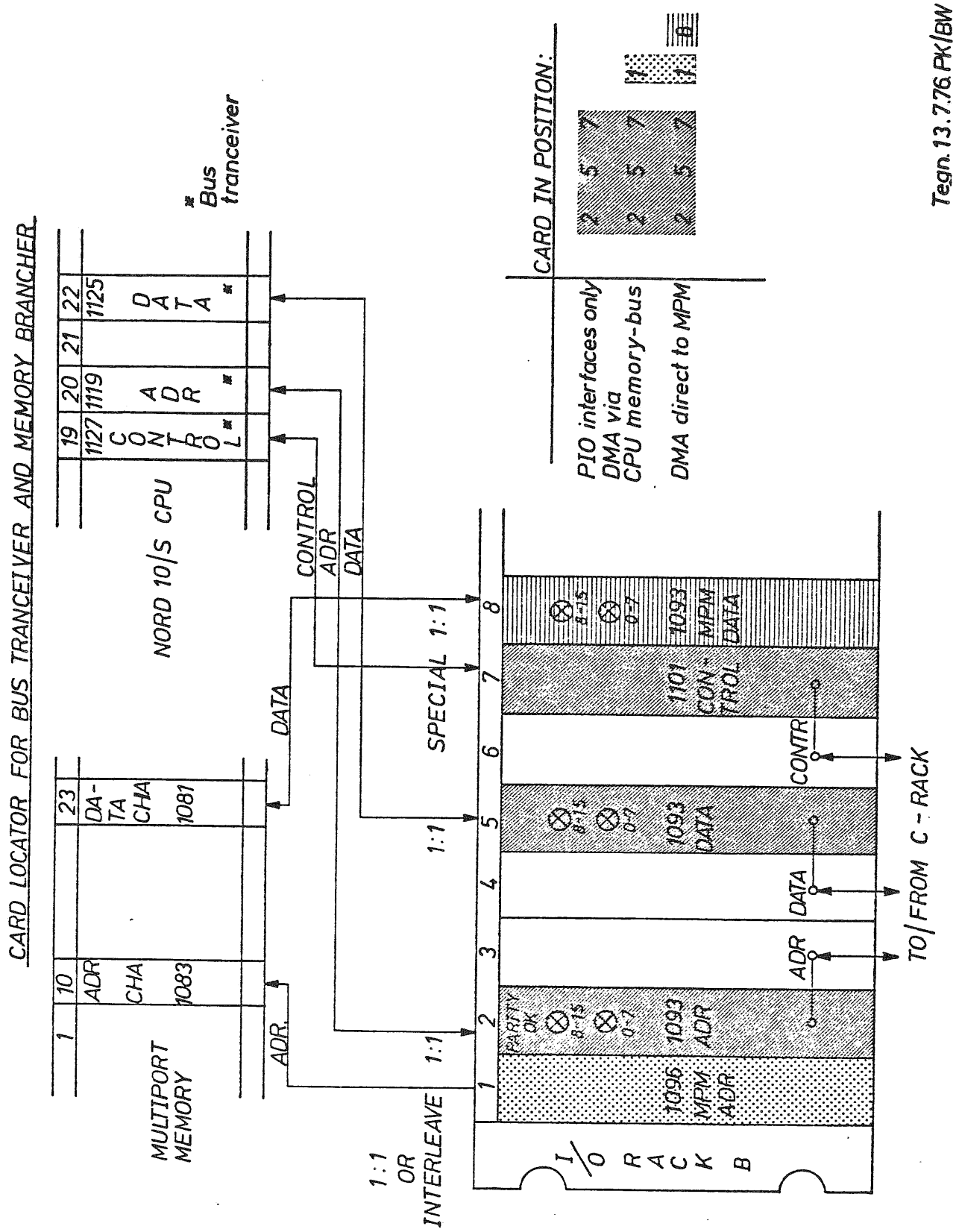
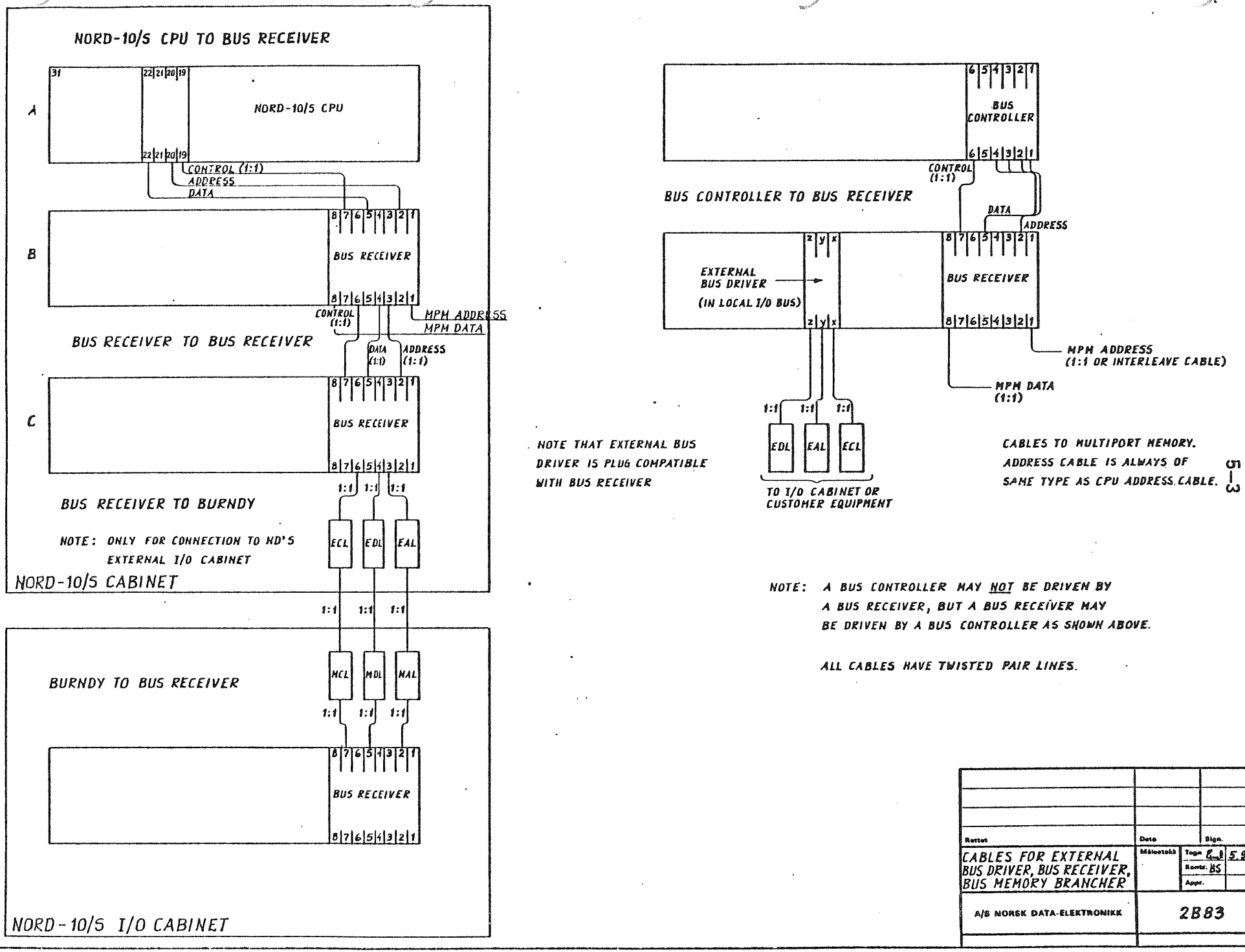


Figure 5.1: CARD LOCATOR FOR BUS TRANSCEIVER AND MEMORY BRANCHER

Figure 5.2: CABLES FOR EXTERNAL BUS DRIVER, BUS RECEIVER, BUS MEMORY BRANCHER



Rettet	Dato	Sign.
CABLES FOR EXTERNAL BUS DRIVER, BUS RECEIVER, BUS MEMORY BRANCHER	Målestokk	Tegn. GJ 5.9.75 Kontr. BS Appr.
A/S NORSK DATA-ELEKTRONIKK	2B83	

5.2 *BUS-RECEIVER/MEMORY-BRANCHER MODULES:*

1093 BRANCH TRANSCEIVER: The 1093 module is an universal card containing:

— Differential line drivers/receivers 18 bits (MO-M17).

— 2 sets of 16 bits tristate drivers driving the output of the differential line receiver.

— 2-1 line selector, selecting the input to the differential line driver.

— Byte-parity generator/checker. Read parity error will turn off light in light-emitting diode and inhibit Data Ready, giving CAR error after a DMA transfer.

NB! The parity generator/checker is only active when writing/reading 18 bits data. (Position 8).

The usage of the circuits mentioned above will depend on the position of the 1093 module.

1096 DMA ADDRESS: The 1096 module contains the 16 Memory Address Registers also called Core Address Register (CAR). The CAR-register is selected by switch-setting on the BUS-CONTROL module 1022, being part of the DMA interface, located in the local I/O bus. One CAR-register for each 1022 module.

1101 BRANCH CONTROL: This control module must always be present (POS 7) and will perform the following functions when:

1. PROGRAMMED I/O INTERFACES IN THE LOCAL I/O RACK:

— Driving/receiving the control-signals between the MAIN and LOCAL I/O BUS.

— Generate control-signals for the data and address flow on the 1093 modules.

— Generate oscillator-signals to the TERMINAL-BUFFER interfaces.

— Generated local IDENT (BIDENT) or external IDENT (EIDENT) signals.

2. DMA INTERFACES IN THE LOCAL I/O RACK:

— Driving the DMA control signals (REQUEST and WRITE) onto the MAIN I/O BUS if a DMA transfer via CPU or onto the multiport-memory lines if a DMA transfer direct to a separate port in the multiport memory-system.

— Generate control-signals for the DMA data and address flow on the 1093 and 1096 modules.

— Detection of request-signals generated in the local rack. If local request; generate BGRANT. If external request, generate OUTGRANT.

On the following drawings the usage of the modules for the different sorts of data flow will be shown. In addition the signals generated on the BRANCH CONTROL 1101 module will be pointed out and explained.

In Figure 5.6 a BUS RECEIVER/BRANCHER data flow overview is given.

5.3 PROGRAMMED INPUT/OUTPUT

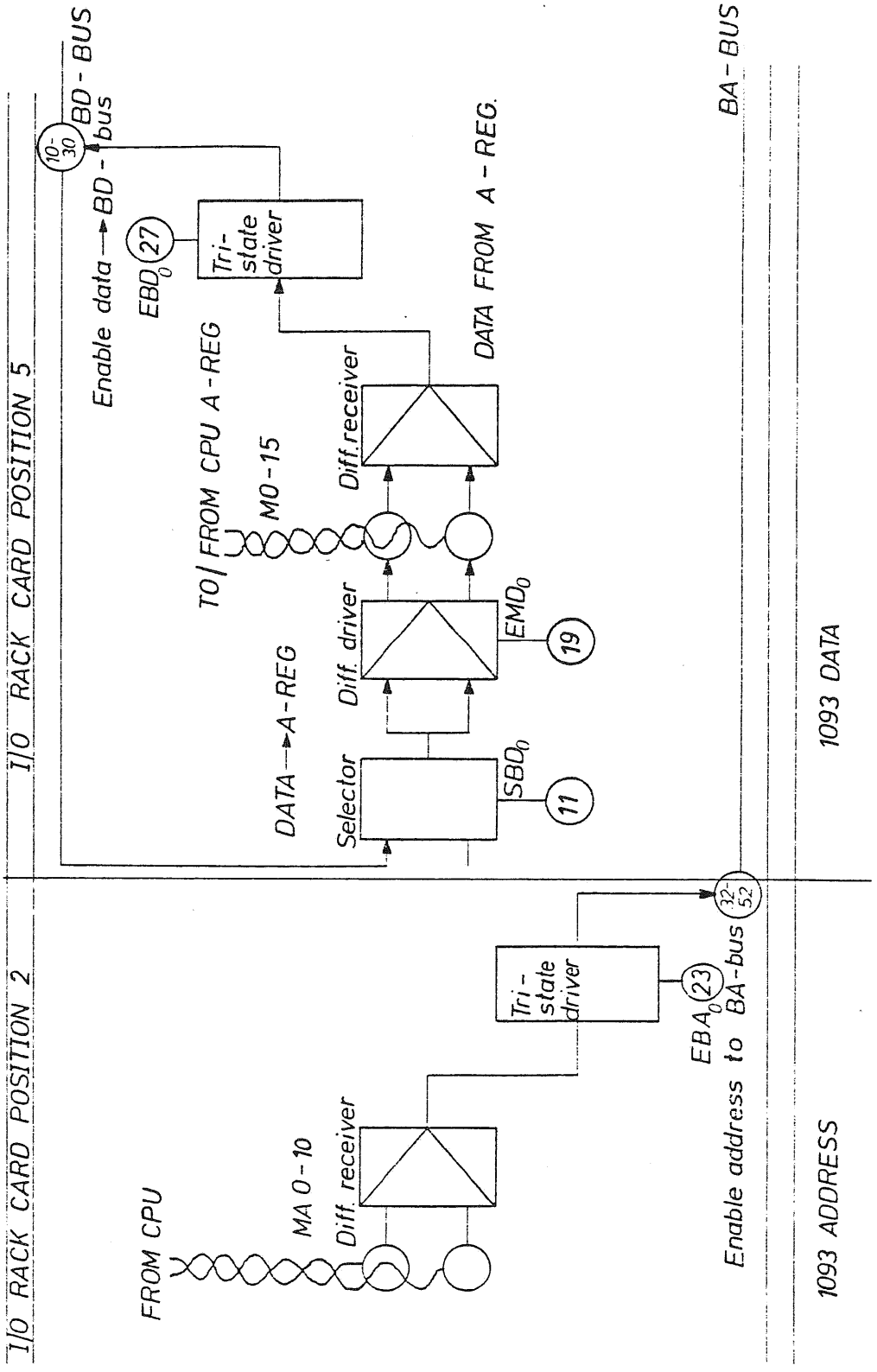
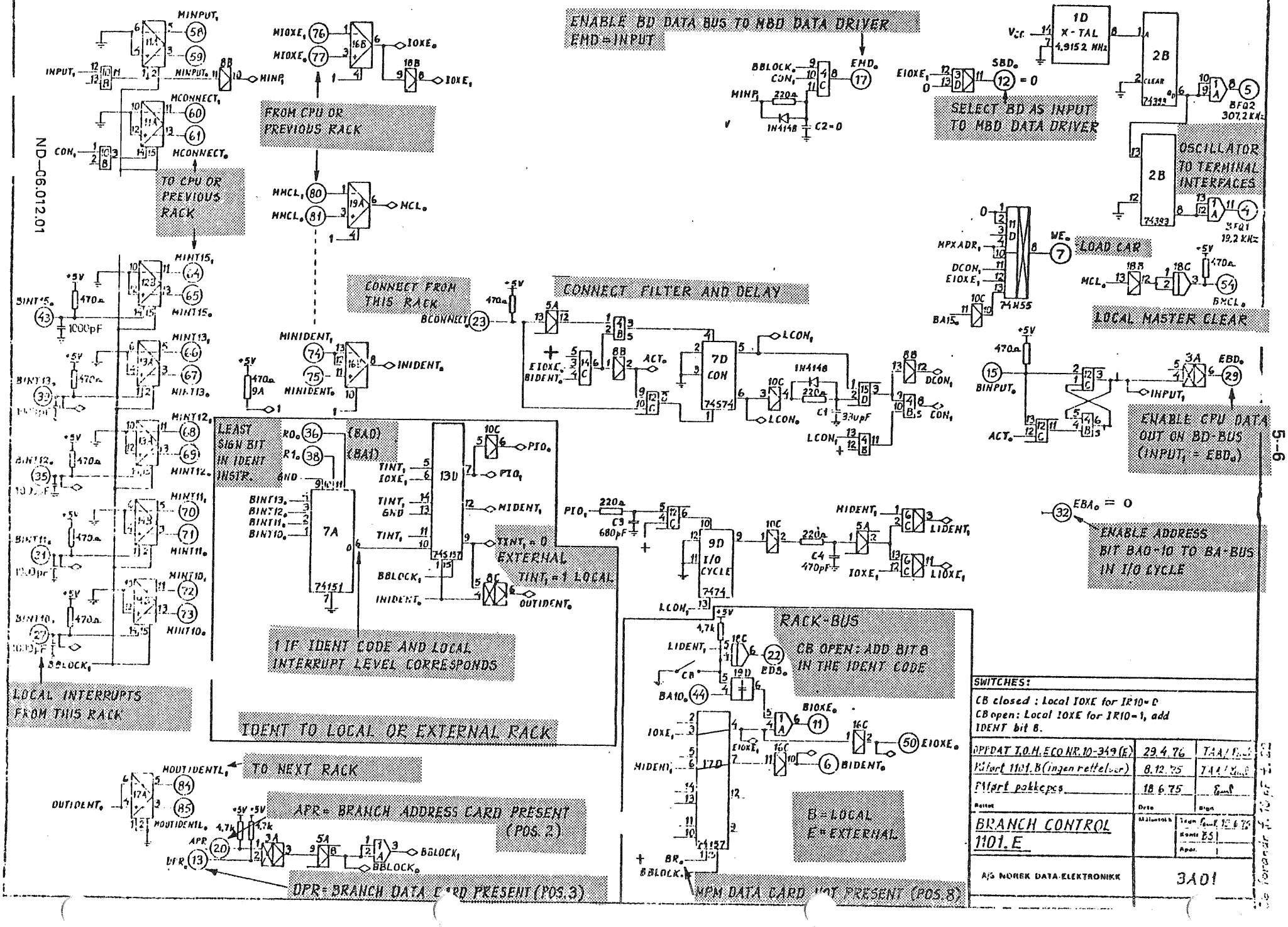


Figure 5.3: PROGRAMMED I/O PIO DATA FLOW

PIO PROGRAMMED I/O



5.4 DMA via CPU and MAIN I/O BUS

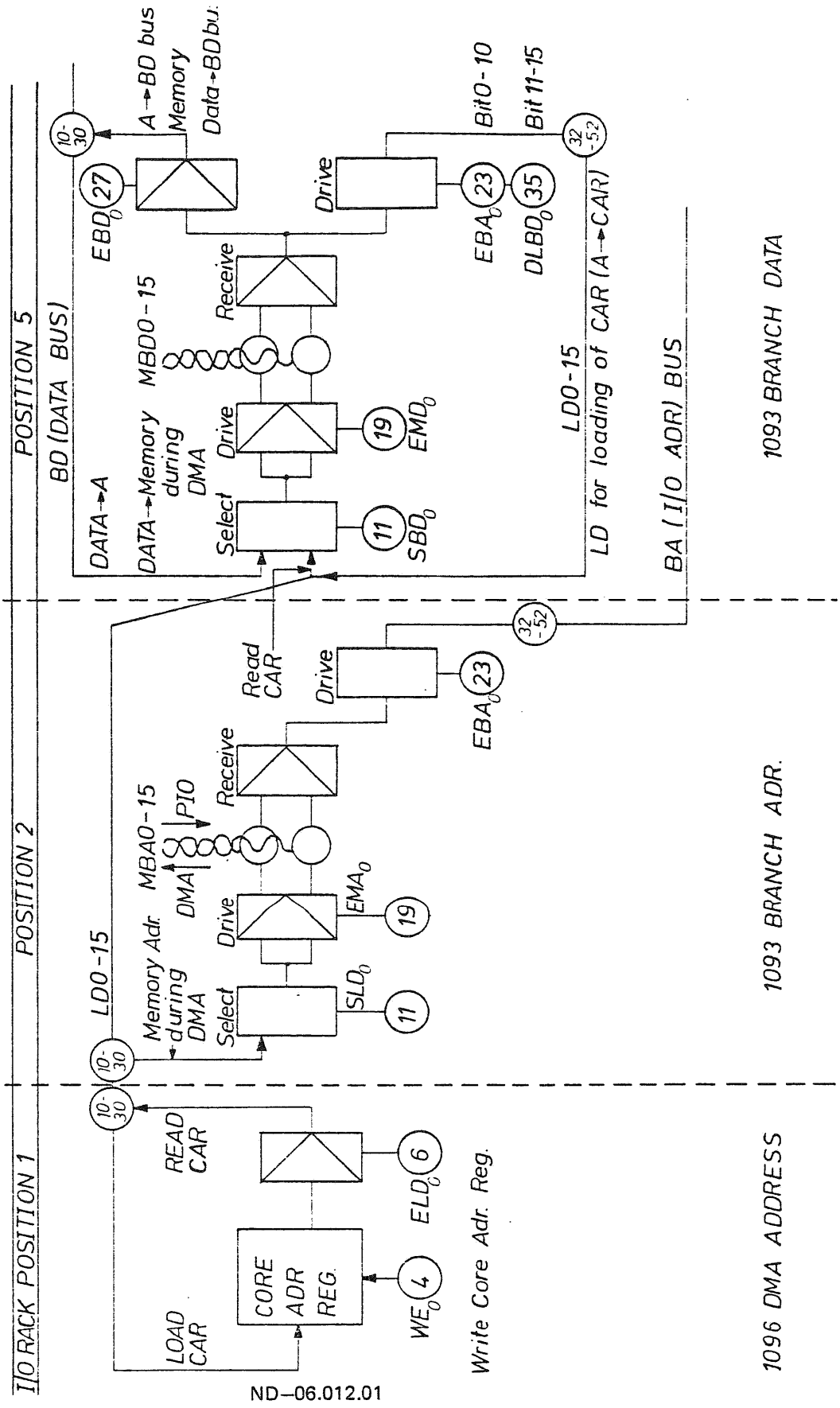
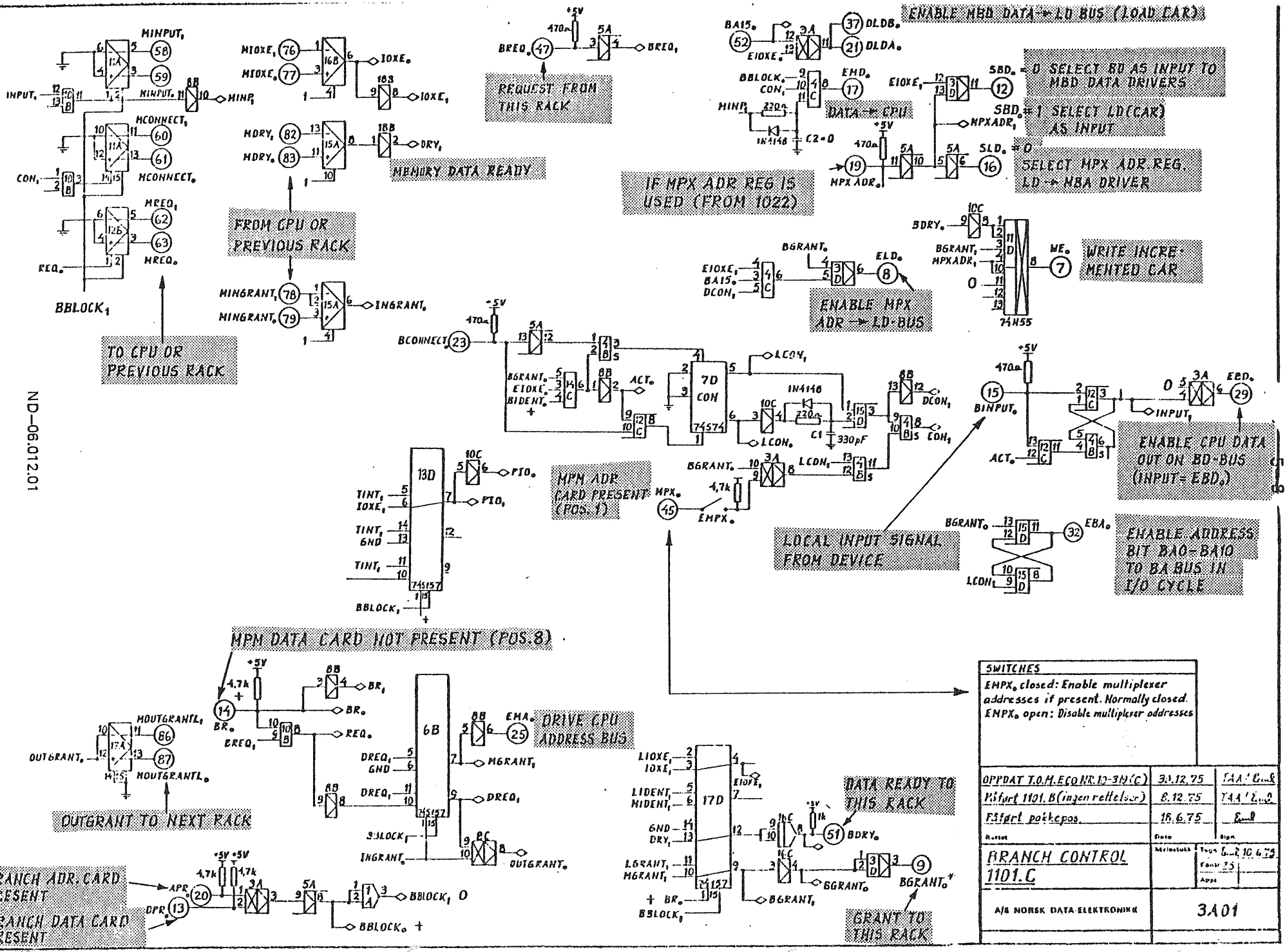


Figure 5.4: DMA TRANSFER VIA CPU DATA FLOW

Tegn. 16.7.76 PK/BW


ENABLE MBD DATA → LD BUS (LOAD CAR)
REQUEST FROM THIS RACK
FROM CPU OR PREVIOUS RACK
MEMORY DATA READY
TO CPU OR PREVIOUS RACK
BBLOCK1
IF MPX ADR REG IS USED (FROM 1022)
SBD0 = 0 SELECT 80 AS INPUT TO MBD DATA DRIVERS
SBD0 = 1 SELECT LD(CAR) AS INPUT
SELECT MPX ADR.REG. LD → MBA DRIVER
DATA → CPU
WRITE INCREMENTED CAR
ENABLE MPX ADR → LD-BUS
ENABLE CPU DATA OUT ON BD-BUS (INPUT = EBD0)
LOCAL INPUT SIGNAL FROM DEVICE
ENABLE ADDRESS BIT BA0-BA10 TO BA BUS IN I/O CYCLE
MPM ADR CARD PRESENT (POS. 1)
MPM DATA CARD NOT PRESENT (POS.8)
DRIVE CPU ADDRESS BUS
DATA READY TO THIS RACK
GRANT TO THIS RACK
OUTGRANT TO NEXT RACK
BRANCH ADR. CARD PRESENT
BRANCH DATA CARD PRESENT
ND-06.012.01
SWITCHES
EMPX0 closed: Enable multiplexer addresses if present. Normally closed.
EMPX0 open: Disable multiplexer addresses
OPPDAT T.O.M.ECO NR.13-3N(C) 30.12.75 TAA
Rifort 1101.B(ingen rettelser) 8.12.75 TAA
Rifort pokkepos. 16.6.75
BRANCH CONTROL 1101.C
A/S NORSK DATA ELEKTRONIKK
3A01

5.5 DMA TRANSFER DIRECT TO/FROM MULTIPORT

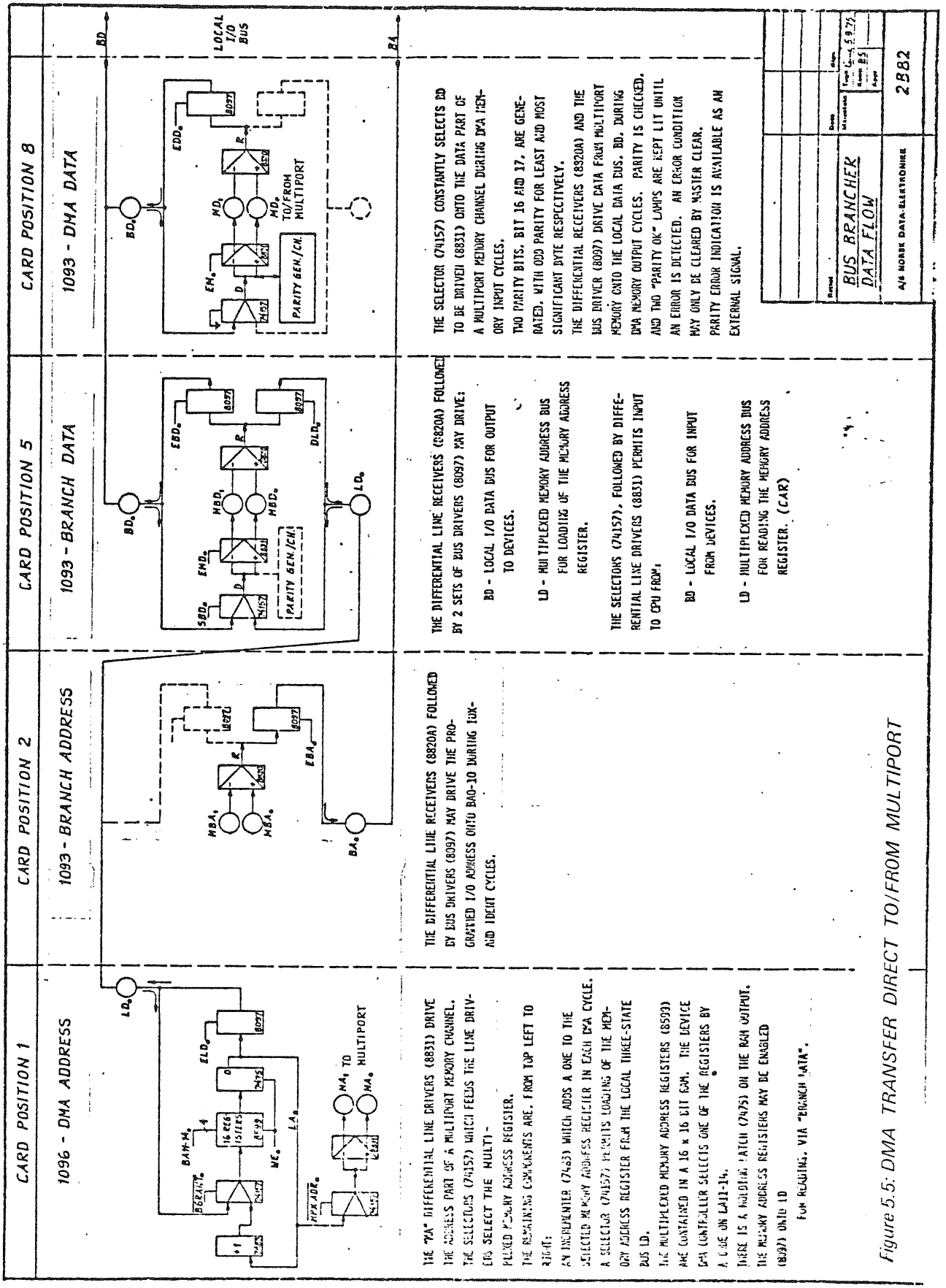
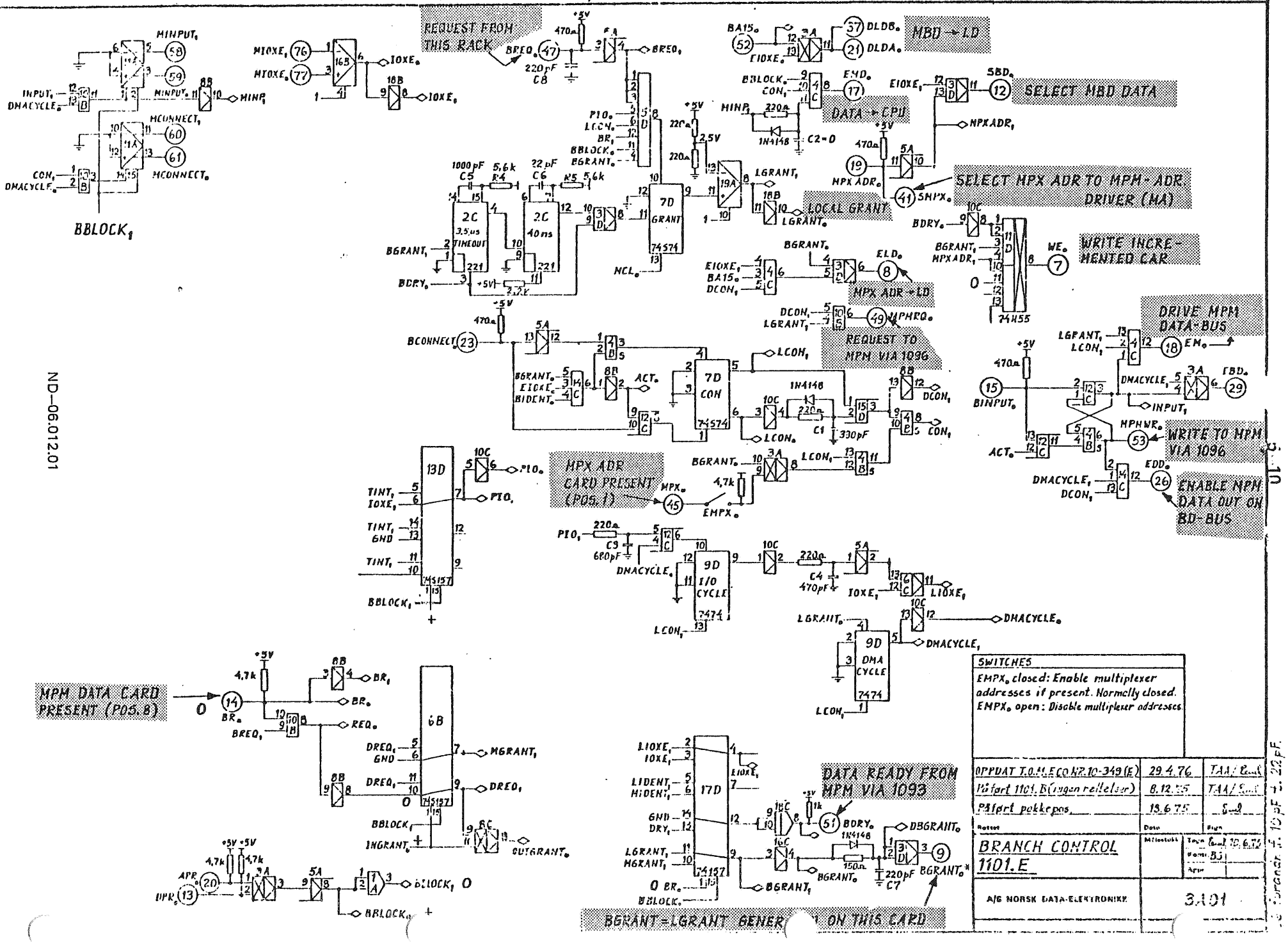


Figure 5.5: DMA TRANSFER DIRECT TO/FROM MULTIPORT

DMA TRANSFER DIRECT TO/FROM MULTIPORT



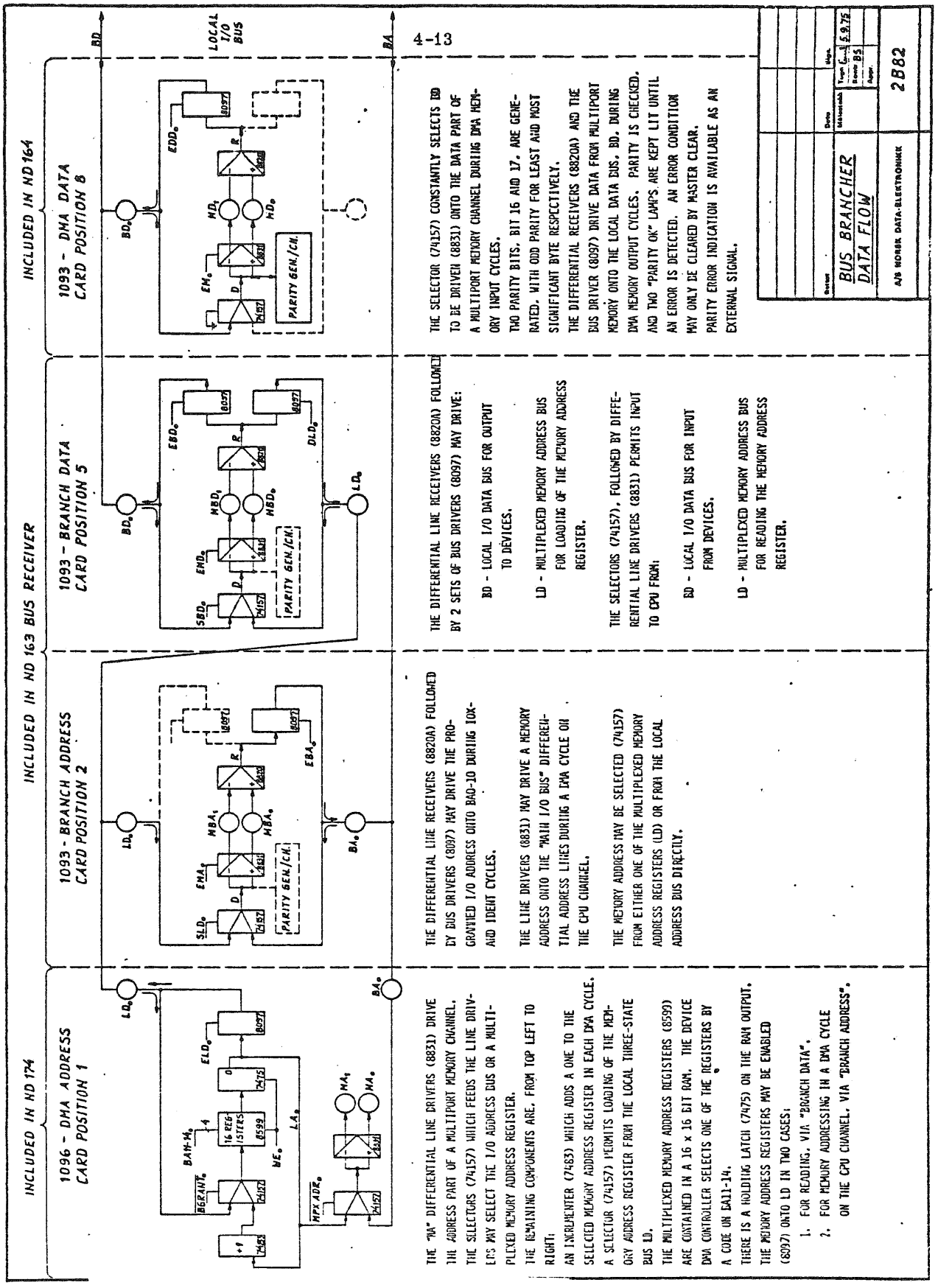


Figure 5.6: BUS BRANCHER DATA FLOW

5.6 *DISCONNECTING THE LOCAL I/O BUS*

The Local I/O bus is easily disconnected from the Main I/O bus. This is done simply by pulling out either the 1093 DATA board in position 5 or the 1093 ADDRESS board in position 2.

With one of the modules outdrawn, the BLOCK-signal on the BRANCH CONTROL is generated with the following effects:

- All local CONTROL signals are disabled from the Main I/O control bus (BBLOCK).
- All local DATA-bits are disabled from the Main I/O data bus (EMD).
- All local ADDRESS-bits are disabled from the Main I/O address bus (EMA).
- The local REQUEST signal is stopped.

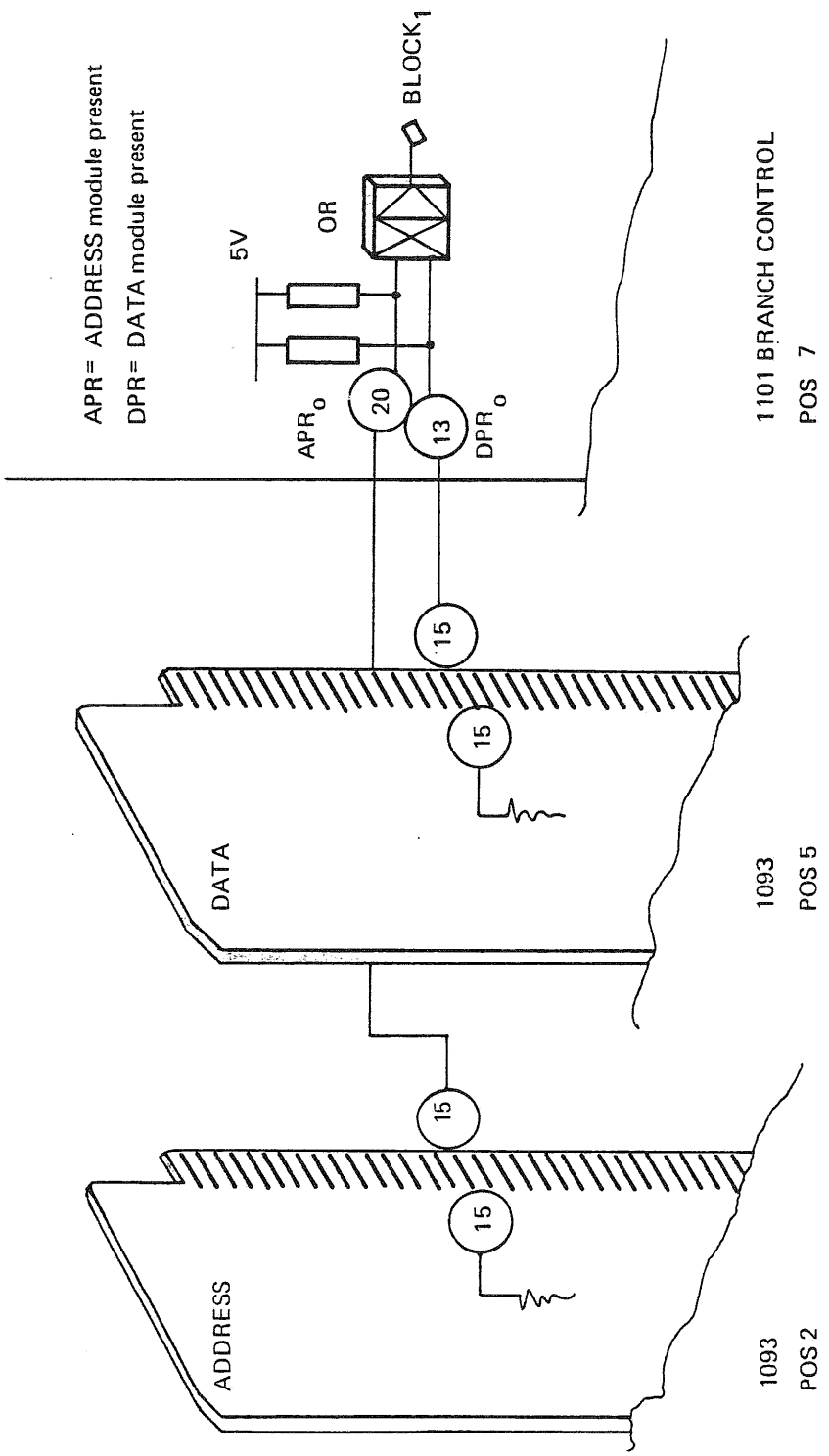


Figure 5.7: BLOCK SIGNAL GENERATION

6 DIRECT MEMORY ACCESS (DMA)

This chapter will deal with the hardware modules involved in a DMA transfer and how a DMA transfer is put through.

6.1 *GENERAL*

A Direct Memory Access-channel is used to obtain high transfer rates to and from main memory. The DMA channel is either connected to main memory via the Main I/O Bus on a CPU cycle steal basis or for higher performance on a separate port in the Multiport Memory System. More than one DMA device may be active on the DMA channel at the same time, sharing the channel's total bandwidth.

The DMA transfer may be divided into three steps:

1. Initialization of the transfer
2. DMA transfer
3. Check the quality of the transfer

Step 1 is executed by means of IOX Programmed Output instructions. Transfer parameters are loaded into various registers in the DMA interface.

Typical:

—The Core Address Register (CAR)
Holds the first memory address to be written into or read from.

—The Block Address Register (BAR)
Holds the first address on the physical-device to be written into or read from (Not used on Mag-tapes).

—The Word Count Register (WC)
The number of 16 bits words to be exchanged between the DMA-device and memory.

—The Control Word Register (CW)
The device operation (read,write,compare..), mode of operation (test), unit number to operate on, interrupt enabling and DMA transfer inialization is set here.

Step 2

During step two the data transfer takes place. Between the interface and device on serial or byte form and between memory and the interface on word basis. Two of the registers are updated dynamically as each word is exchanged between the interface and memory. The Word Count Register is decremented, and the Core Address Register is incremented.

Step 3

The quality of the transfer is verified by reading various registers by means of IOX-instructions.

Typical:

– The Status Register (STS)
  Errors occurring during the transfer betweeen Memory←→Interface and between Interface←→Physical Device are found here.

– The Core Address Register (CAR)
  At the end of the transfer this register should keep the address of the last referred memory location. CAR (AT END OF TRANSFER) - CAR (AT START OF TRANSFER) = WC (WORD COUNT).

  By reading this register it is also possible to calculate the number of bytes in a mag-tape record with unknown record length.

DMA TRANSFER IN THREE STEPS

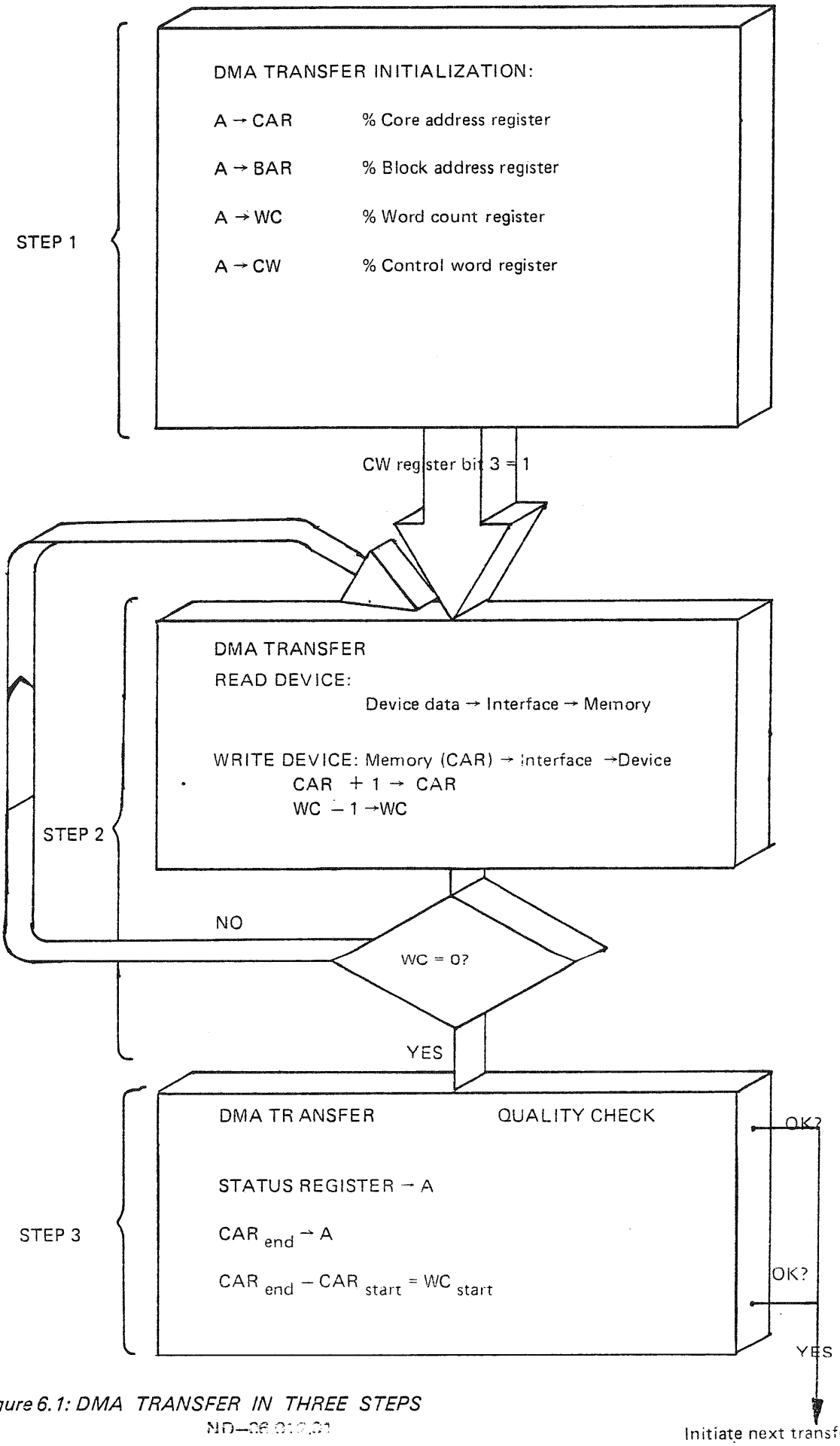


Figure 6.1: DMA TRANSFER IN THREE STEPS

6.2 *IOX FORMAT*

IR-register format during an IOX instruction transferring data to/from a DMA device register:

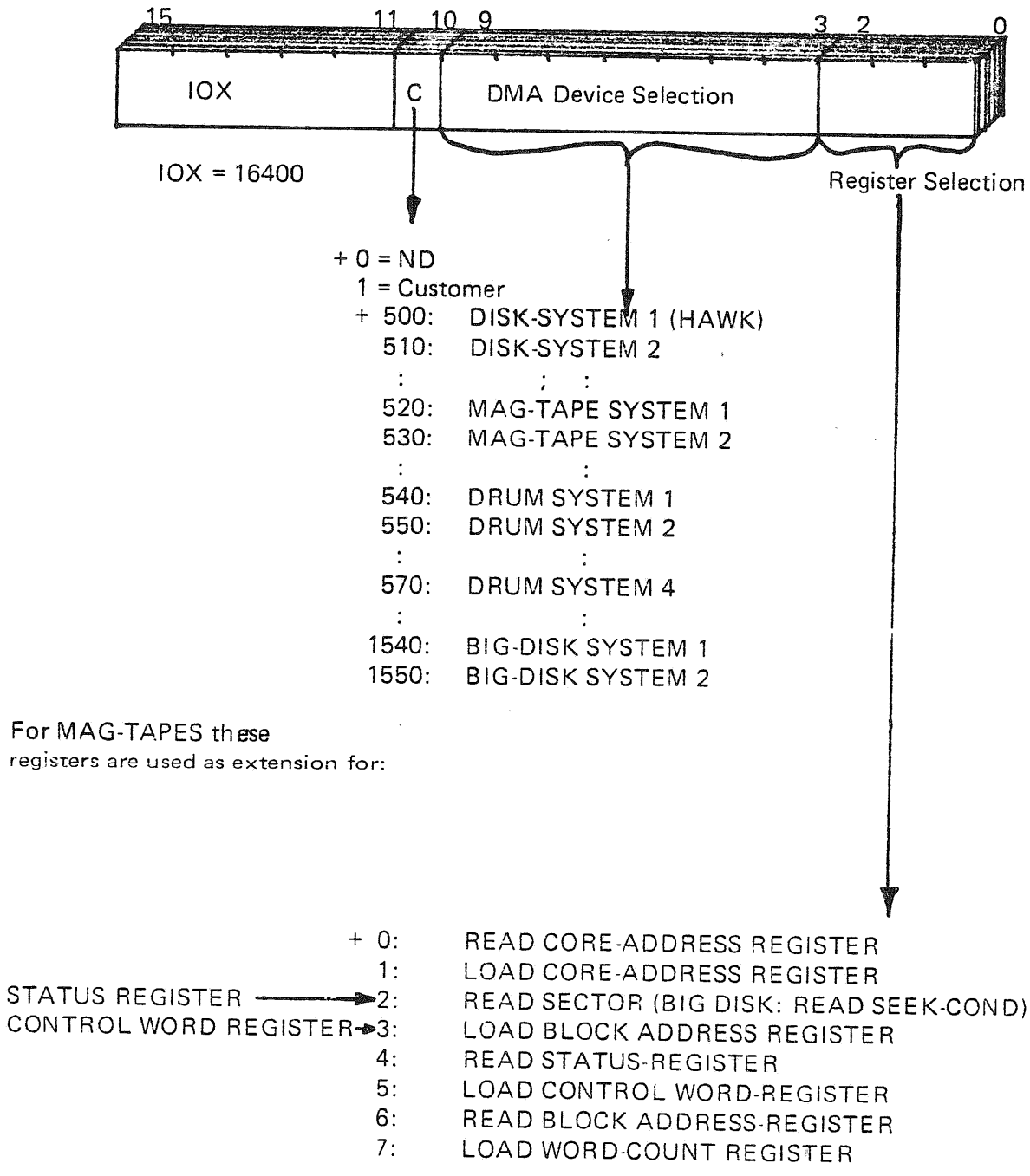
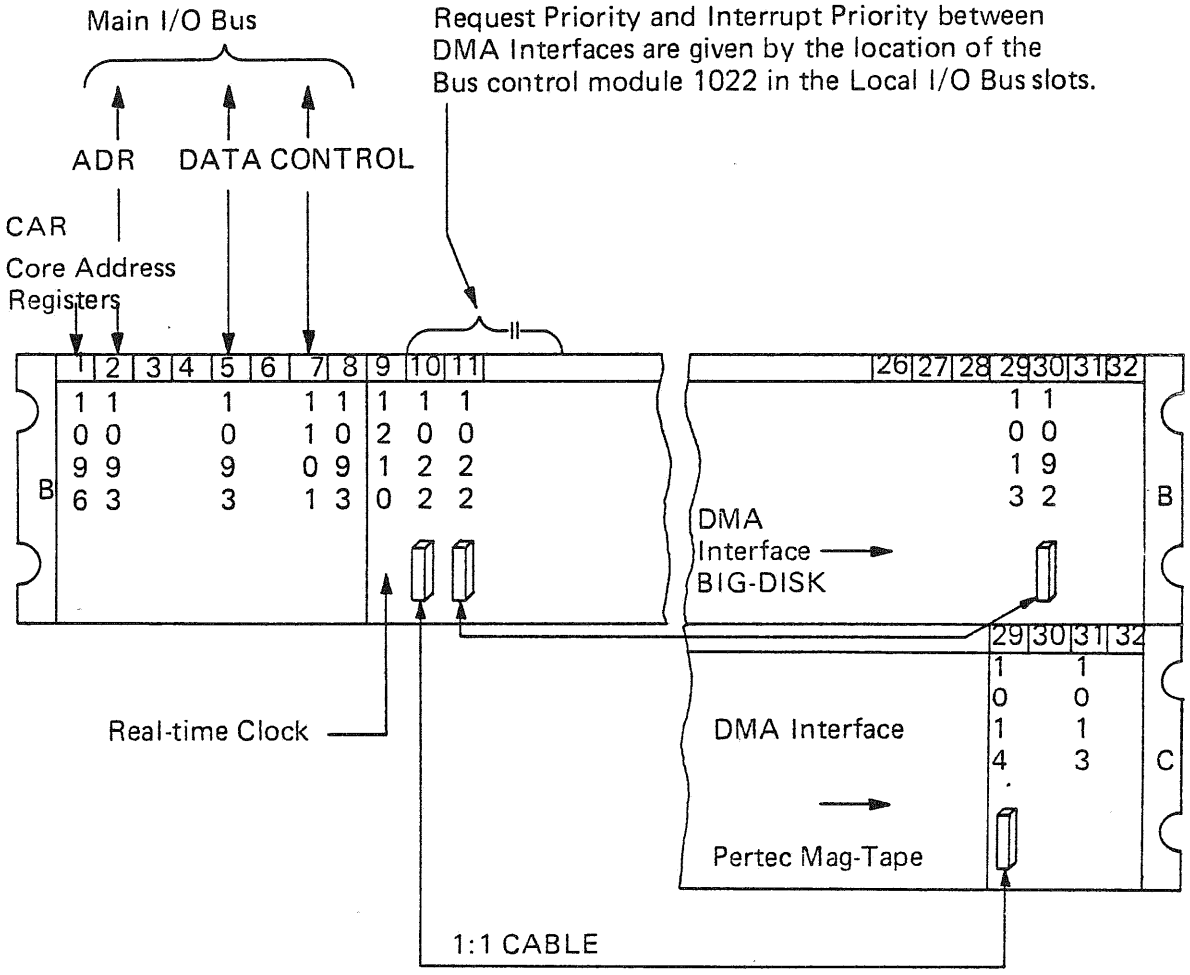


Figure 6.2:

6.3 *INTERFACE ORGANIZATION:*



For details see drawing 7.4

1014 DMA Register
1092 Bufferred DMA Register (including 64 words buffer)
1129 DMA Register (including overrun detection)

} WORD COUNTER – WC

1013 Device Registers

} BLOCK-ADDRESS BAR REGISTER

Figure 6.3: DMA INTERFACE ORGANIZATION

6.4 *CORE ADDRESS REGISTER (CAR)*

The Core Address Register is located on the DMA ADDRESS module 1096. This module is always located in I/O rack slot 1. Refer also to figure 6.4.

The 16 CAR-registers are contained in 4 integrated circuits (8599, 4x4 Register files) with 4 bits in each. The CAR-register to be selected is given by switches/straps on the 1022 module. The switch setting is enabled on the address lines BA 11-14 by each CONNECT-signal generated on the specific 1022 module.

The rule is that the 1022 module being closest to the DMA ADDRESS module should have the lowest CAR number.

During initialization the A-register; now on LDO-15 lines is selected as input to the addressed CAR-register (no GRANT signal present). During DMA transfer the 16 bits CAR register is incremented on each DATA-READY pulse from memory. The addressed and latched CAR register is added with one (forced carry) and written back in the same address (GRANT signal present). To make an 18 bits DMA address the CAR register is extended by two bits in the Control Word Register (Bit 5 and 6). These two bits are used as BANK-SELECT bits BA 16 and 17. ADDRESS bits 16 and 17 will remain static during the complete transfer while ADDRESS bits 0-15 will be counting pr. word.

The signal MPX-ADR = Multiplexed Address is generated on the 1022 module, selecting the multiplexed address as address lines to memory.

For the customer, taking care of the Core Address himself, the second half of the address-selector on the 1093 and 1096 module is available (BA 0-15) (No MPX ADR signal generated).

The memory address is sent direct to multiport via the 1096 module (Position 1) or via the MAIN I/O BUS through the 1093 module (Position 2).

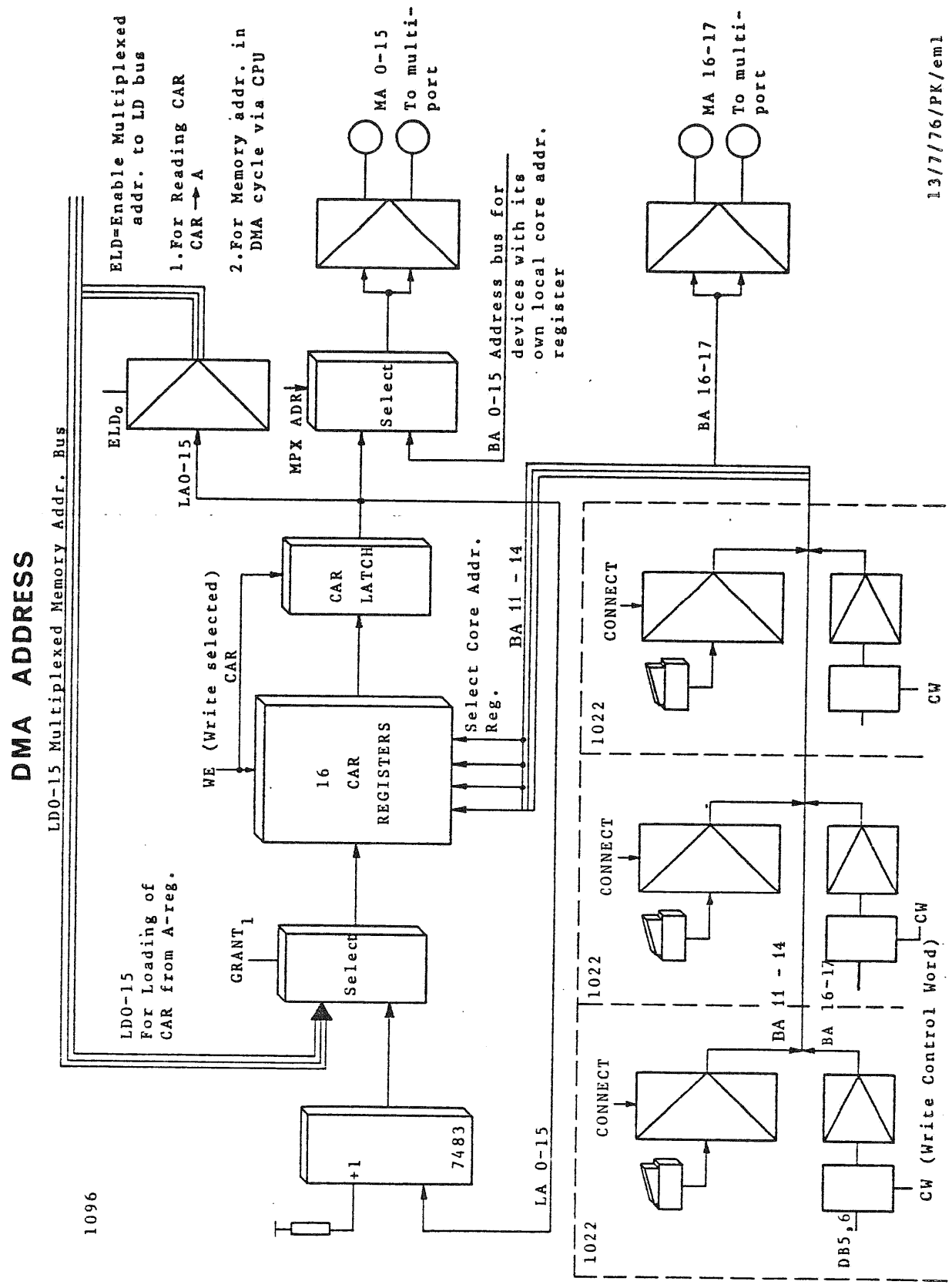
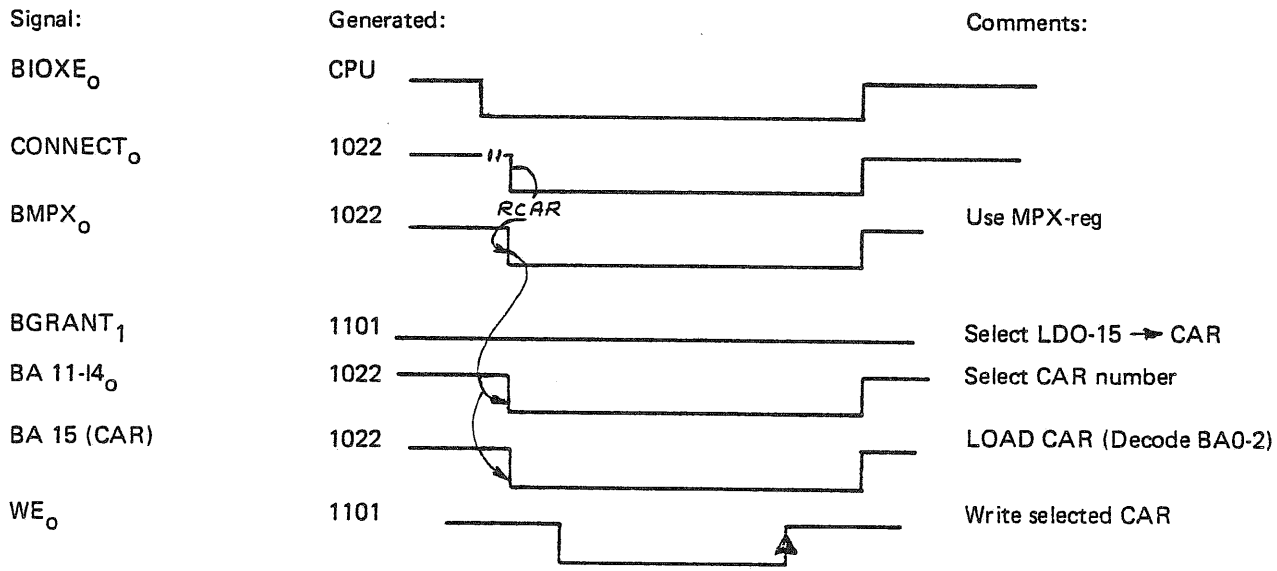


Figure 6.4: DMA ADDRESS

1. LOAD MULTIPLEXED CORE-ADDRESS REGISTER
   (IOX LOAD CAR)



2. INCREMENT MPX-CAR during DMA

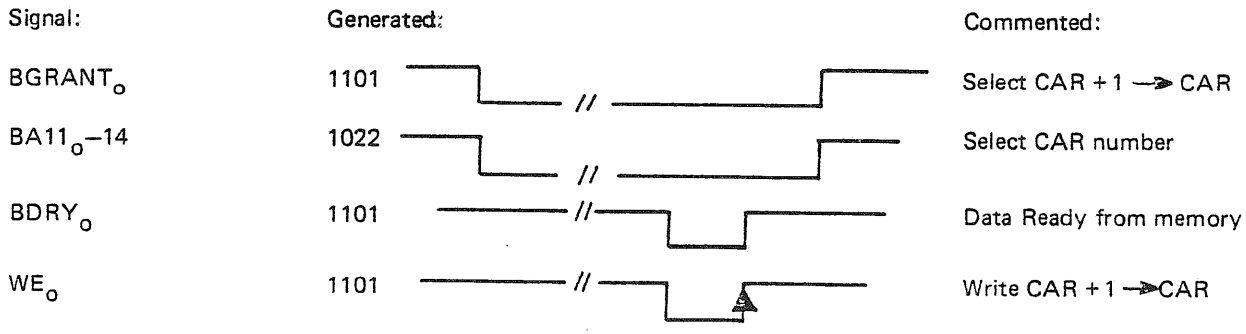


Figure 6.5: LOAD MPX-CAR (IOX LOAD CAR)

6.5 *BLOCK ADDRESS REGISTER (BAR)*

The 16 bits Block Address Register is located on the DEVICE REGISTER module 1013 and contains the physical address of the device. The content of this register is unchanged during the data transfer.

As an example the BAR-register format of the CDC HAWK and BIG-DISK is shown:

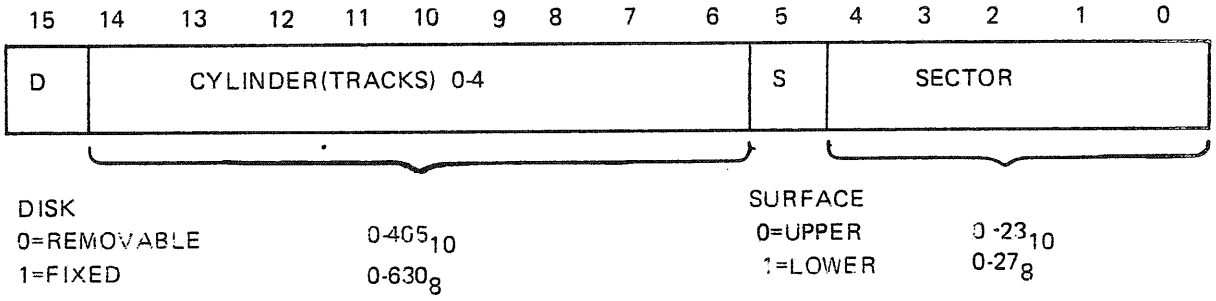
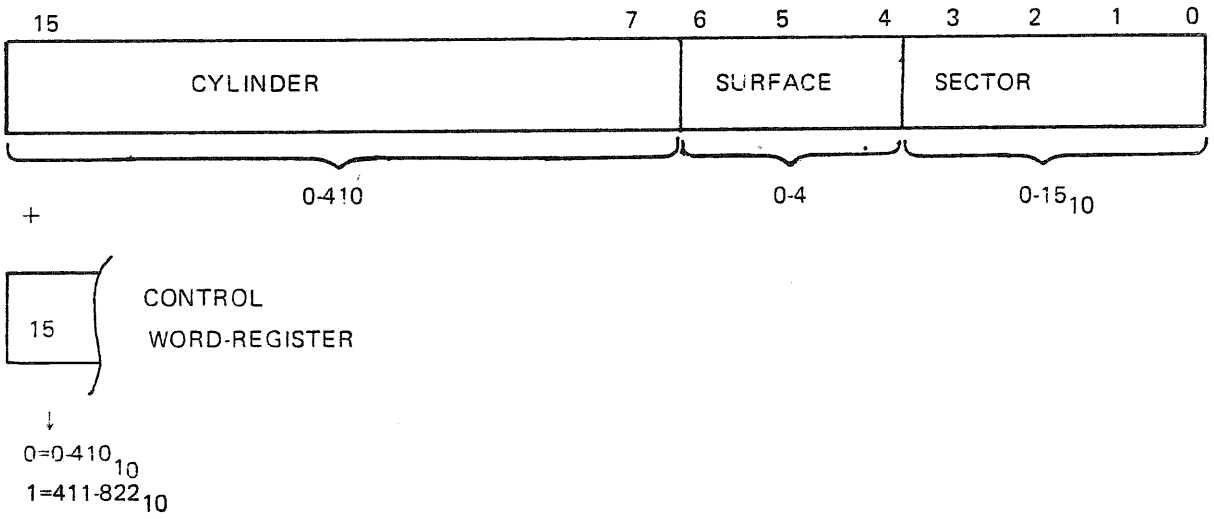


Figure 6.6: HAWK DISK:



CDC BIG DISK:

6.6 *DMA-DATA TRANSFER ON MAIN I/O BUS*

The time from the START signal (BD2.CW) to the exchange of data between the interface and memory starts is device dependent. For a disk this time is given by the difference between the former head position (disk-address) and the new disk address. For a BIG-DISK the max time = 55ms = maximum positioning time + 17ms = one rotation. Minimum time = 90 μs = time used to read and compare the address.

The following is a list of the MAIN events occuring in a DMA transfer:

1. When the serial bits/parallel bytes are assembled in one word during READ operation or the assembling register is empty during a WRITE operation, a DMA REQUEST signal is generated. The signal passes on the 1:1 cable between the interface and the 1022 module. The DMA REQUEST signal is buffered and ORed on to the LOCAL I/O BUS.

2. As the TRANSCEIVER CONTROL module 1127 in the CPU receives this signal a GRANT signal is returned if:

   A) No IOX or IDENT instruction in progress
   B) The previous DMA-CYCLE has finished

   At the finish-time of these events the GRANT signal is returned.

3. In parallel with returning the GRANT signal to the requesting 1022 module, the signal is used on the 1127 module to allocate the memory address bus BA and data bus BD for a DMA transfer. The GRANT signal will also disable the address lines output from CPU (IREN).

4. The first device to receive the GRANT signal (called OUTGRANT) is the first device in the DMA priority chain represented by the 1022 module. If this module did not generate the DMA REQUEST, it would transmit the INGRANT signal as the OUTGRANT signal from this device. The daisy chaining mechanism for the INGRANT/OUTGRANT signal is identical to the one for INIDENT/OUTIDENT.

5. Finding the requesting 1022 module, this module will return a CONNECT and INPUT signal to the CPU.

   A) If INPUT true: MEMORY WRITE OPERATION
   B) If INPUT not true: MEMORY READ OPERATION

6. The CONNECT signal will enable the switch selectable (BA 11-14) CAR register out on the MAIN I/O ADDRESS BUS.

   If INPUT is true, the assembled data is enabled on the MDB-bus (Bus between the 1022 module and the interface). On the 1022 module the data is enabled out on the LOCAL I/O BUS (BD). On the 1093 module (POS 5) the local data bus is driven onto the MAIN I/O BUS (MO-15). The REQUEST signal is now reset (RRQ).

7. The CONNECT signal together with a GRANT signal will generate a memory request signal BREQ in the TRANSCEIVER CONTROL module 1127. The BREQ signal is sent to memory when the address bus is allocated to the external DMA source (ALBAE).

8. After some time, depending on READ or WRITE, local memory or multiport memory, a ADDRESS READY (BAR) and MODULE DATA READY (BDR) will turn up. BDR is approximately 120 ns after BAR if READ.The BAR signal will set IDLE, clocking new requests (if any) appeared while the DMA REQUEST was in progress. Memory Ready (MRD) equal BDR if WRITE and delayed 150 ns if READ will generate the EXTERNAL FINISH (EFIN) signal. EFIN resets GRANT and the DMA CYCLE ends. Ending the DMA cycle, the next DMA-REQUEST can be treated.

9. The EXTERNAL DATA READY signal equal to EFIN is sent back to the DMA interface via the 1022 module and used to strobe the output data if MEMORY READ.

10. When GRANT turns off, the CONNECT signal is dropped on the 1022 module indicating the MAIN I/O BUS is ready for a new DMA data transfer.

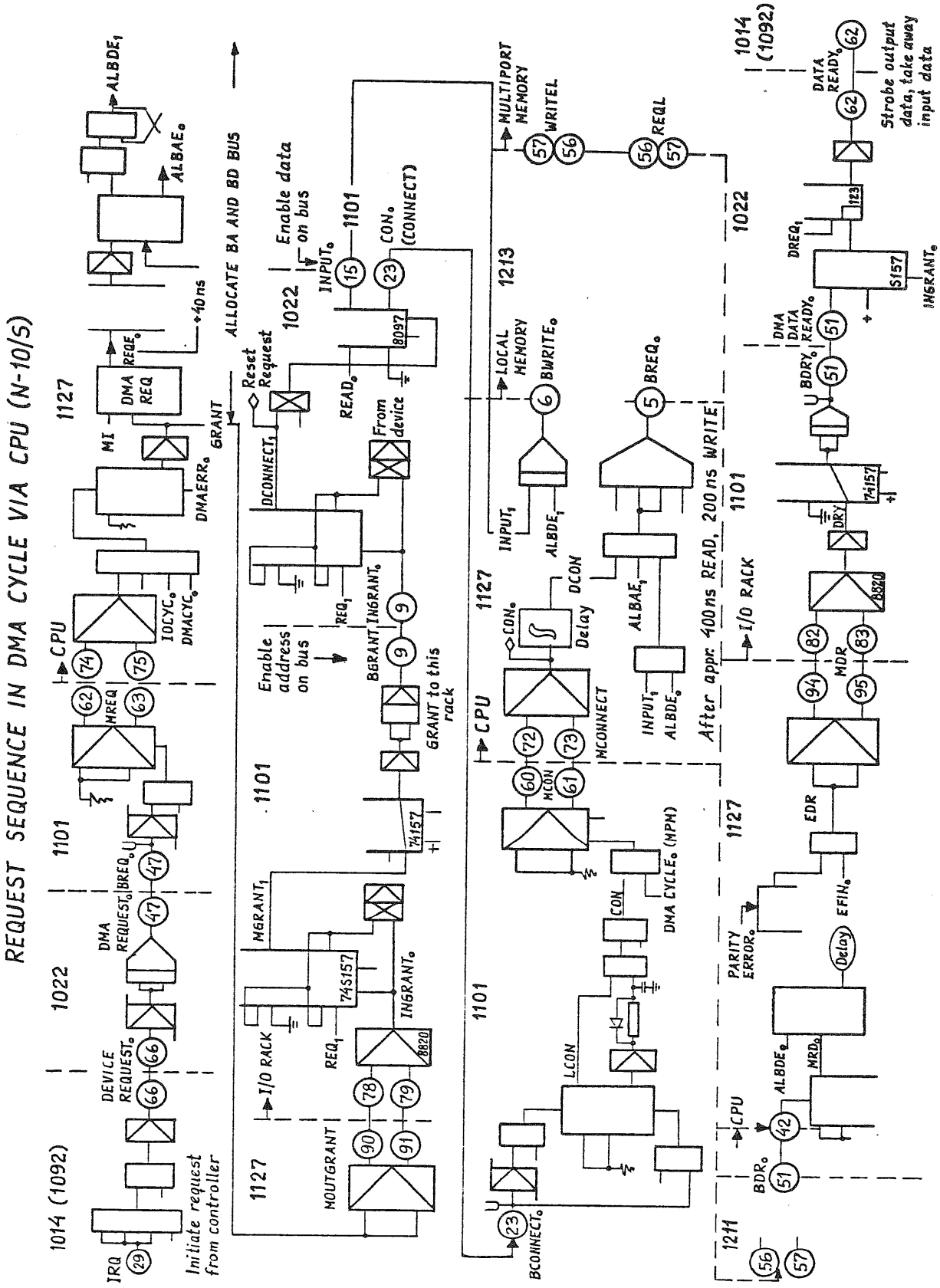


Figure 6.7: REQUEST SEQUENCE IN DMA CYCLE VIA CPU (N-10/S)

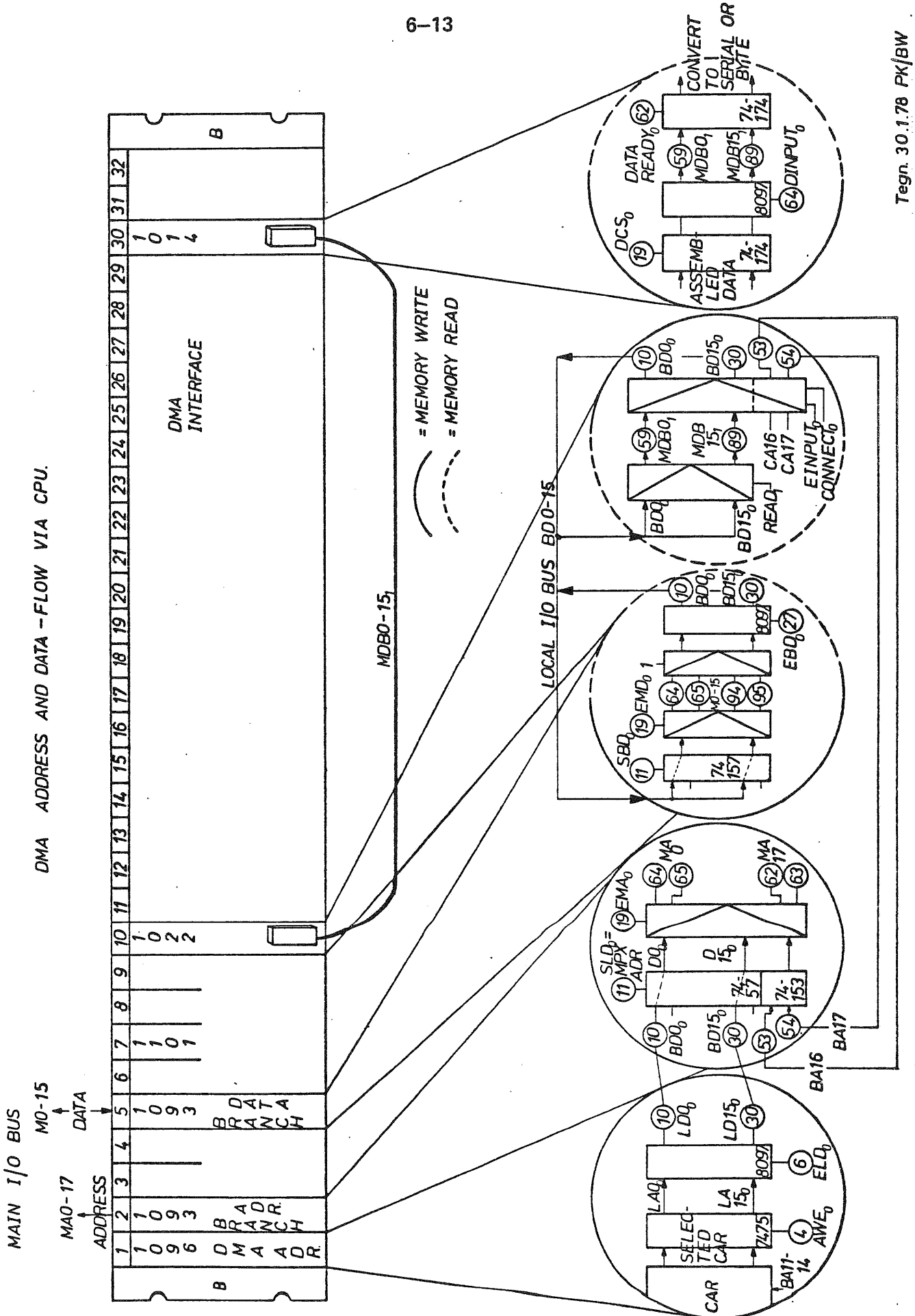
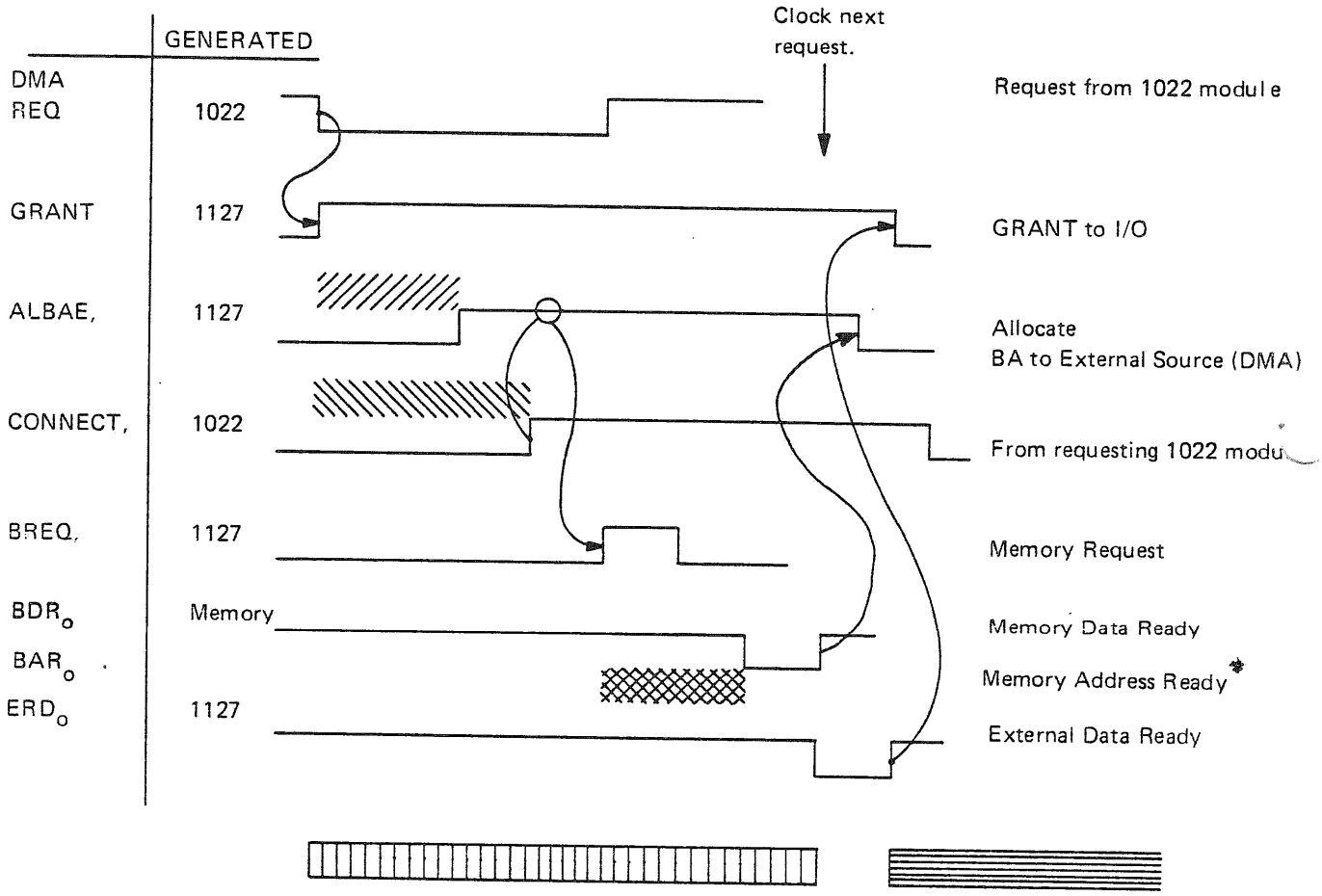


Figure 6.8: DMA ADDRESS AND DATA-FLOW VIA CPU

ND–06.012.01

DMA TIMING DIAGRAMS:

DMA TRANSFER VIA CPU.



* BAR 120 ns before BDR during memory read

Depends on the CPU and REFRESH activity.

Depends upon the number of REQUESTS with higher priority.

Depends on read or write, local memory or multiport memory access

CPU or REFRESH Request appearing in this period will be clocked with the Address-Ready (BAR) signal.

= If NO CPU or REFRESH- requests, the next DMA-request will be handled

Figure 6.9: DMA TIMING DIAGRAMS:

6.7 *DMA TRANSFER IMPROVEMENTS*

When the transfer speed of the device approaches the max DMA speed of the MAIN I/O BUS, two improvements are available. (Max transfer rate via CPU to/from local memory equals one request pr. 1.2μs for READ memory and one request pr. 1.4μs for WRITE memory).

Improvements:

1. A direct multiport channel may be installed where the max transfer rate equals one request pr. 1.0μs.

2. Installing a BUFFERED DMA-REGISTER module 1092. This module contains a 64 words First In-First Out (FIFO) buffer.
   NB! All DMA devices with lower priority then the buffered one, have to use the BUFFERED DMA module, otherwise data will be lost.

6.8 *DMA TRANSFER DIRECT TO/FROM MULTIPORT*

With a 1093 module installed in I/O rack position 8, the following exceptions during the DMA transfer will take place :

- The DMA-REQUEST is disabled from the MAIN I/O BUS on the BRANCH CONTROL 1101 module.
- The GRANT signal is generated on the 1101 module. CPU will never notice the DMA transfer.
- Multiport Memory Request is generated on the reception of the CONNECT signal from the requesting 1022 module and sent to MPM via the 1096 module.
- The Memory DATA READY signal from multiport is routed via the 1093 (POS 8) to the 1022 module.
- Data is routed to/from multiport via the module in position 8.
- Address is sent direct to multiport from the module in position 1.

NB! All REQUESTS from DMA interfaces represented with a 1022 module in this rack will be routed to the Multiport.

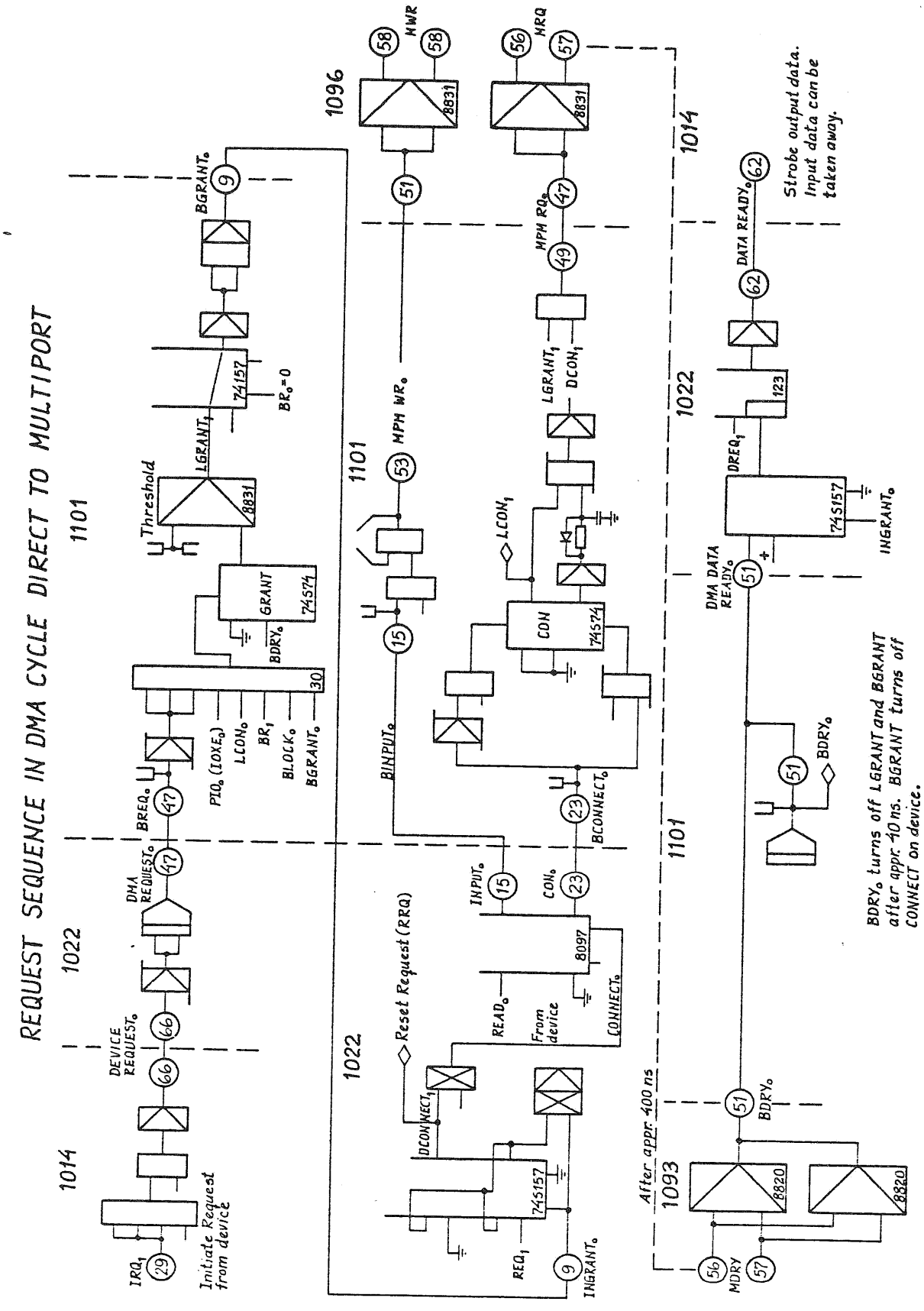


Figure 6.10: REQUEST SEQUENCE IN DMA CYCLE DIRECT TO MULTIPORT

DMA ADDRESS AND DATA-FLOW DIRECT TO/FROM MULTIPORT

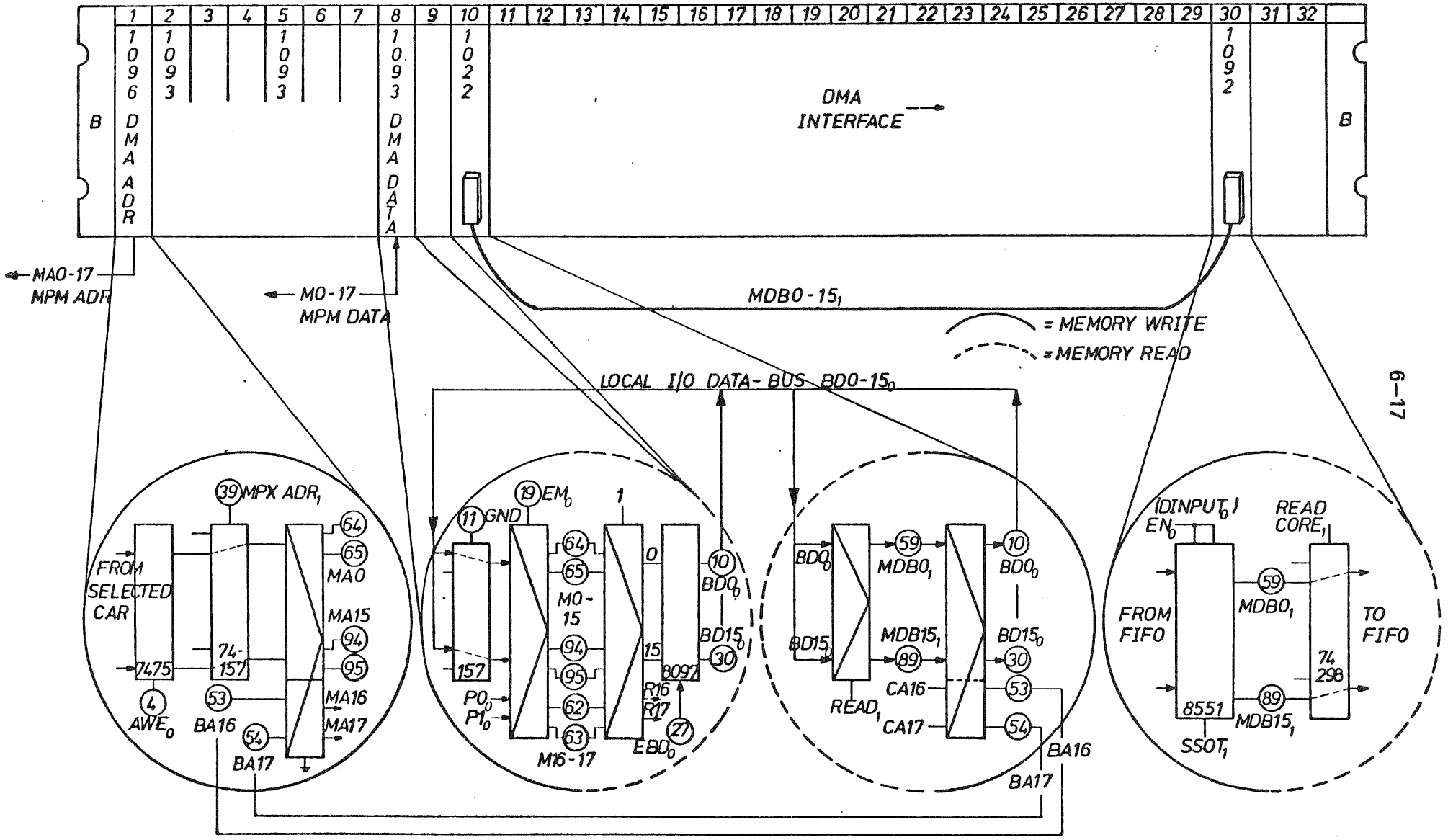


Figure 6.11: DMA ADDRESS AND DATA-FLOW DIRECT TO/FROM MULTIPORT

Tegn. 30.1.78 PK/BW

7 DMA STANDARD MODULES

This chapter will cover the following ND produced DMA standard modules:

1022 BUS CONTROL

1014 DMA REGISTER

1092 BUFFERED DMA REGISTER

7.1 *1022 BUS CONTROL*

The BUS CONTROL module is the communication link between the LOCAL I/O BUS and the DMA Interface containing these main functions:

— IOX-Address Decoding

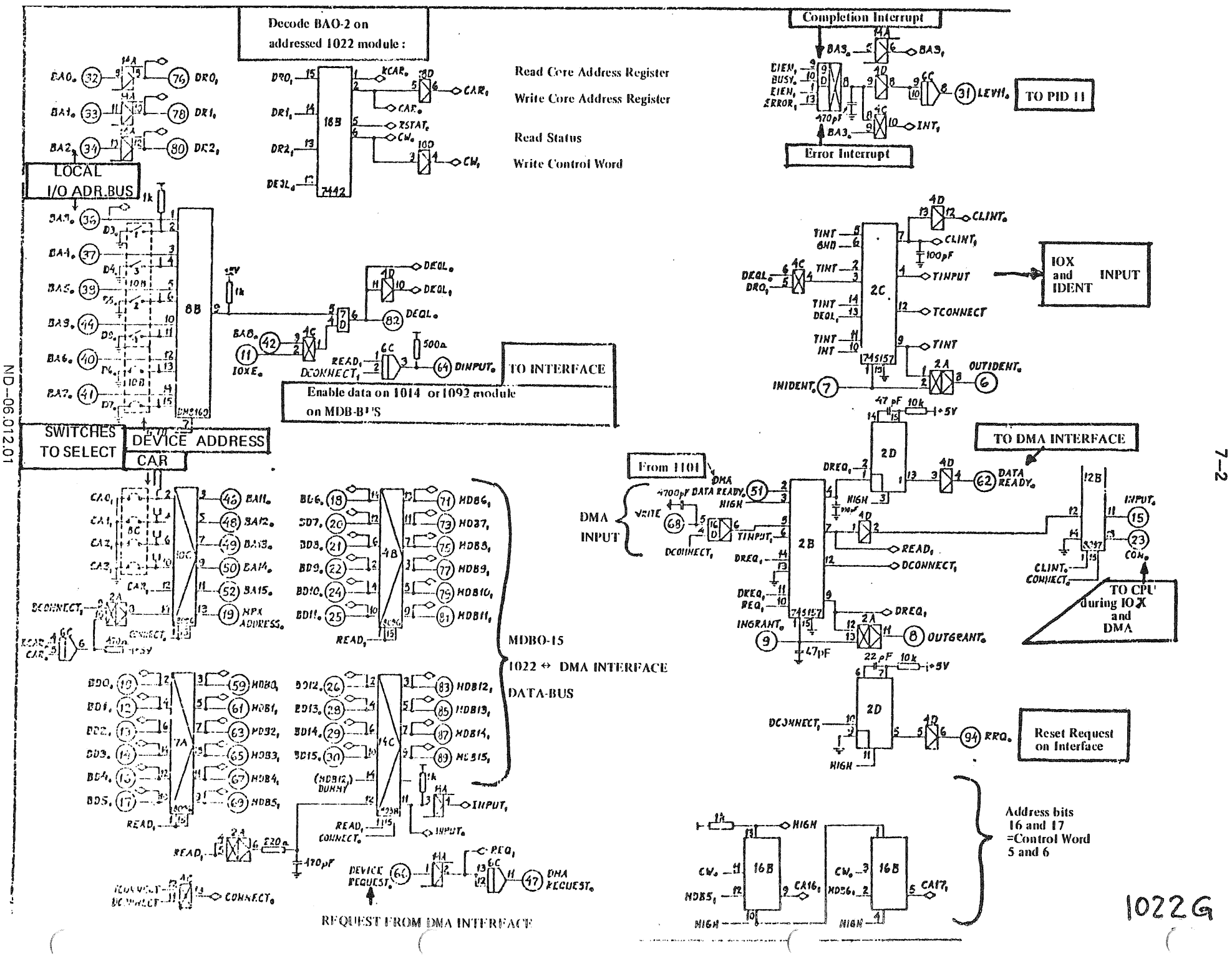
— Core Address Register handling

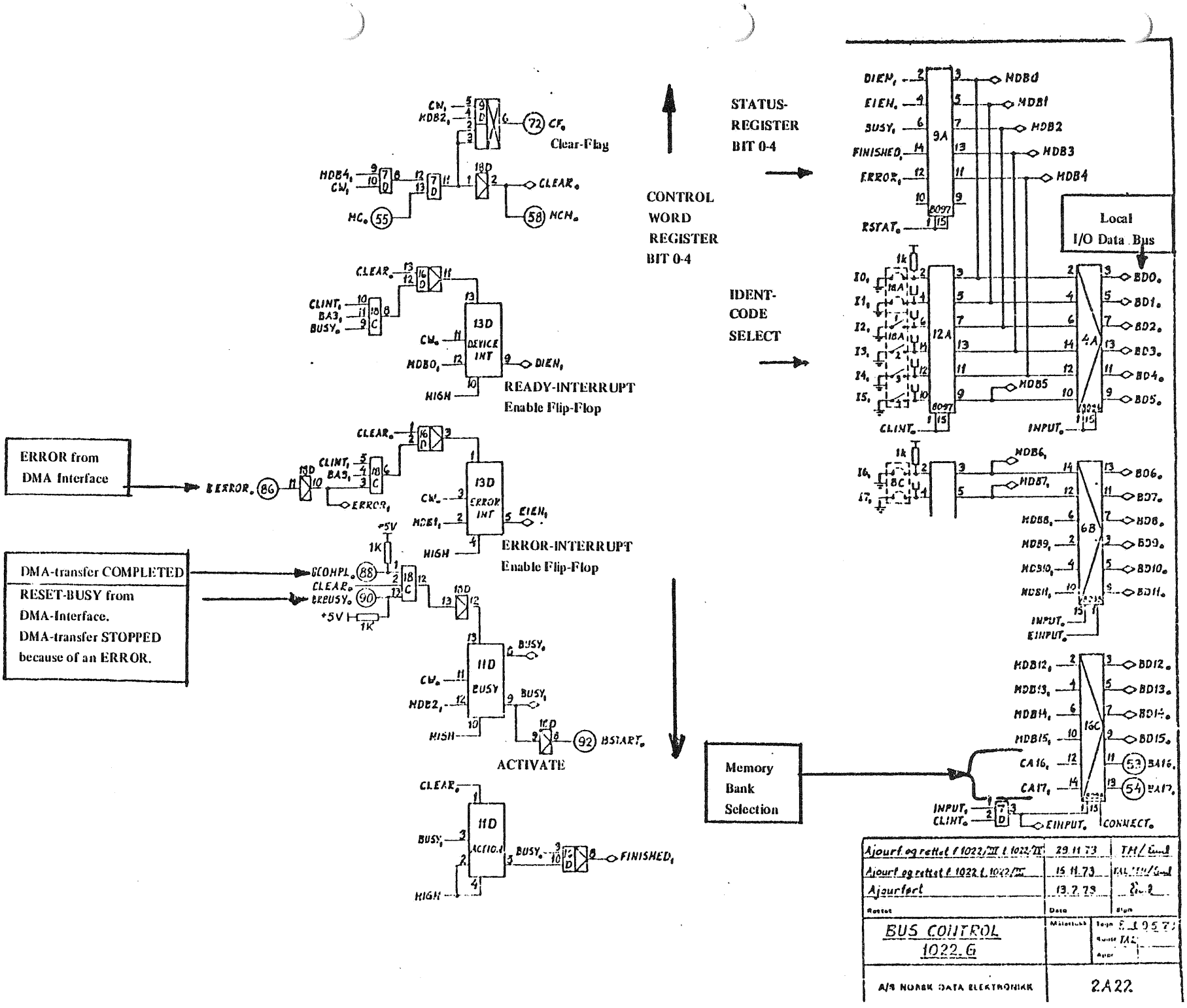
— DMA-INTERRUPT generation

— IDENT mechanism

— REQUEST routing

— GRANT mechanism


Decode BA0-2 on addressed 1022 module :
Read Core Address Register
Write Core Address Register
Read Status
Write Control Word
Completion Interrupt
Error Interrupt
TO PID 11
LOCAL I/O ADR.BUS
SWITCHES TO SELECT DEVICE ADDRESS
CAR
TO INTERFACE
Enable data on 1014 or 1092 module on MDB-B'S
IOX and IDENT INPUT
TO DMA INTERFACE
From 1101
DMA INPUT
TO CPU during IOX and DMA
MDBO-15
1022 ↔ DMA INTERFACE
DATA-BUS
REQUEST FROM DMA INTERFACE
Reset Request on Interface
Address bits 16 and 17 =Control Word 5 and 6
1022G
ND-06.012.01
7-2

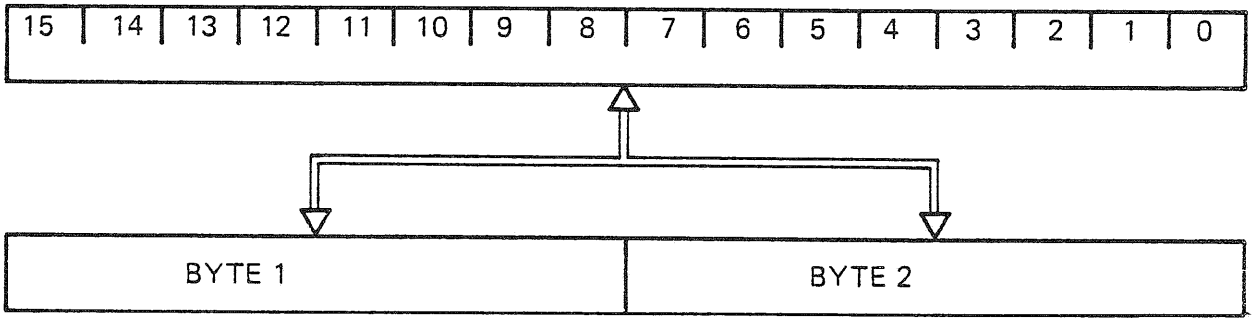

STATUS-REGISTER BIT 0-4
CONTROL WORD REGISTER BIT 0-4
IDENT-CODE SELECT
Local I/O Data Bus
Clear-Flag
READY-INTERRUPT Enable Flip-Flop
ERROR-INTERRUPT Enable Flip-Flop
ACTIVATE
ERROR from DMA Interface
DMA-transfer COMPLETED
RESET-BUSY from DMA-Interface.
DMA-transfer STOPPED because of an ERROR.
Memory Bank Selection
DEVICE INT
ERROR INT
BUSY
ACTIV.
CONNECT
A/S NORSK DATA ELEKTRONIKK
BUS CONTROL
1022.G
2A22

7.2 *DMA REGISTER 1014*

The 1014 module performs the following functions:

- Convert a 16 bits word to two 8 bits byte
- Convert two 8 bits bytes to a 16 bits word

Bit Number:



- Serial to parallel conversion during device READ
- Parallel to serial conversion during device WRITE
- Generate "Device Request"
- Word Counter
- Word counter equals zero detection

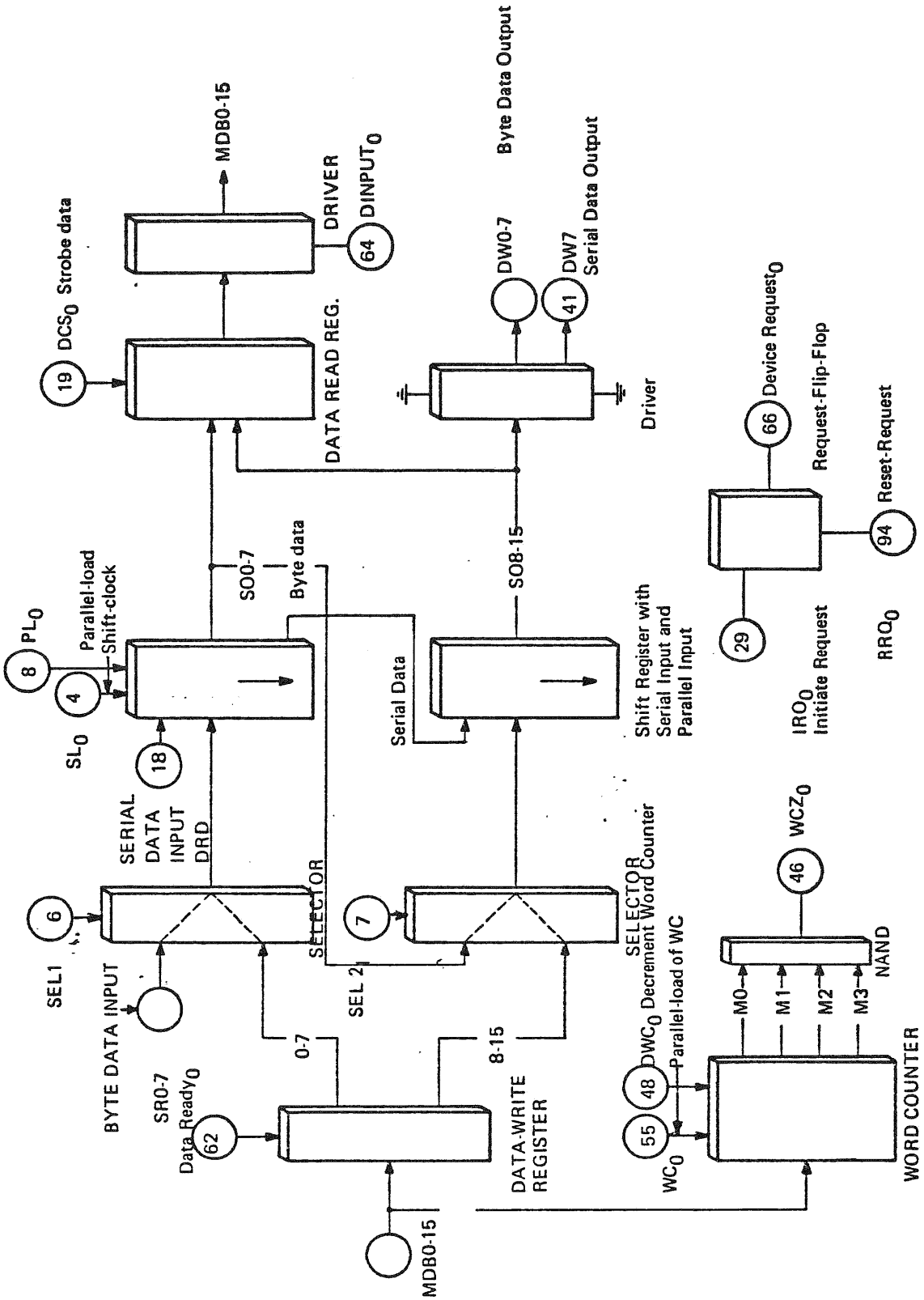


Figure 7.1: BLOCK DIAGRAM-DMA REGISTER 1014

7.3 *BUFFERED DMA REGISTER 1092*

The 1092 module performs the following functions:

- First In-First Out (FIFO) asynchronous buffer register of 64 words + control network
- Shift register - 16 bits assembly/disassembly*
- Generate "Device Request"*
- Word Counter*
- Request Counter
- Word counter equal zero detection*
- Request counter equal zero detection
- Status bit 11 generation (DMA failure, OVERRUN)

*These functions are identical within the 1014 module.

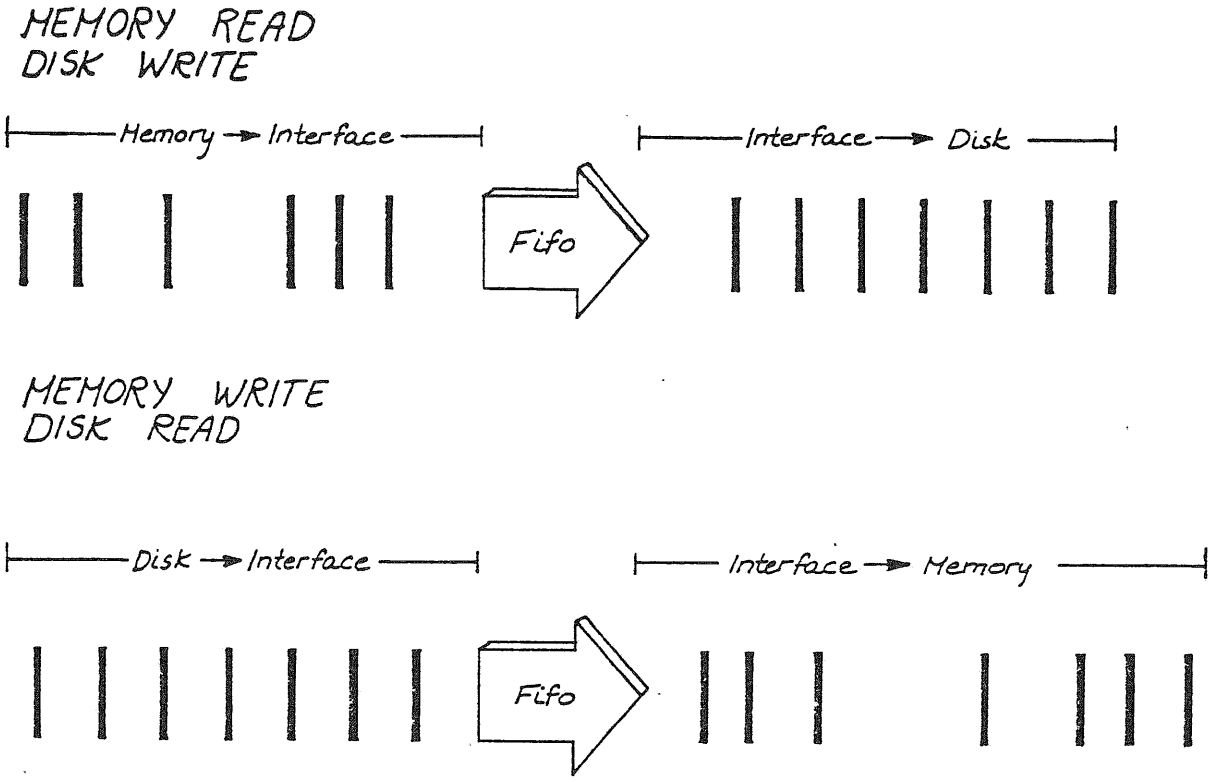


Figure 7.2: FIFO PRINCIPLES

7.3.1 *BUFFERED DMA REGISTER 1092 DESCRIPTION*

FIFO INPUT SELECTOR/LATCH (Refer to *Figure 7.3*).

READ CORE	=	READ CORE signal active will select the MDBO-15 data from the 1022 module as input and the data will be latched at DATA READY (DRY,CLB) time. During WRITE CORE the assembled word SO-15 will be selected as input and latched

64 WORDS FIFO

IR	Input Ready: The first bit position is empty and data can be inputted on a shift in (SI) command
SI	Shift in data when Input-Ready is true
OR	Output Ready: Presence of valid data on the output pins
SOT	Shift one word of data out when Output Ready is true

Shifting data through an empty FIFO will take approximately 15μs.

BUS DRIVER

The data shifted out of the FIFO DO-15 is clocked with the Shift Output command. The latched data is enabled out on the tristate MDBO-15 bus when the the DINPUT signal arrives from the 1022 module (DINPUT = WRITE MEMORY.CONNECT)

ASSEMBLING/DISASSEMBLING CIRCUITS

PL	= Parallel load of shift register
SL	= Shift pulse
DRD	= Serial data input
S15	= Serial data output
SRO-7	= Byte Input to be ASSEMBLED
S8-15	= DISASSEMBLED byte output
SEL1,SEL2	= Selects input to shift register. SEL1≠SEL2 only during byte/word assembling, disassembling

WORD COUNTER (WC)

WCS	= Word Counter Strobe Parallel load of the WORD-COUNTER. Loaded with MDBO-15 = A-register bits 0-15 during an IOX WC instruction.
DWC	= Decrement WC The WC-register is decremented at Initial Request (IRQ) time. The WORD-COUNTER keeps track of the words handled by the physical device (BIG-DISK).

REQUEST-COUNTER (RC)

WCS	= See WORD COUNTER
RRQ	= Reset Request The request counter (RC) is decremented with the RRQ signal. The RRQ signal is generated on the 1022 module as a reply signal of the request. The REQUEST-COUNTER keeps track of the number of words handled by the memory. The difference between the Request Counter and the Word Counter should then be the words buffered in the FIFO.
SB 11	DMA error During MEMORY READ: The FIFO goes empty; no output ready (OR) During MEMORY WRITE: The FIFO goes full; no input ready (IR)

During WRITE CORE the Word Counter will reach ZERO before the Request Counter.

During READ CORE the Request Counter will reach ZERO before the Word Counter.

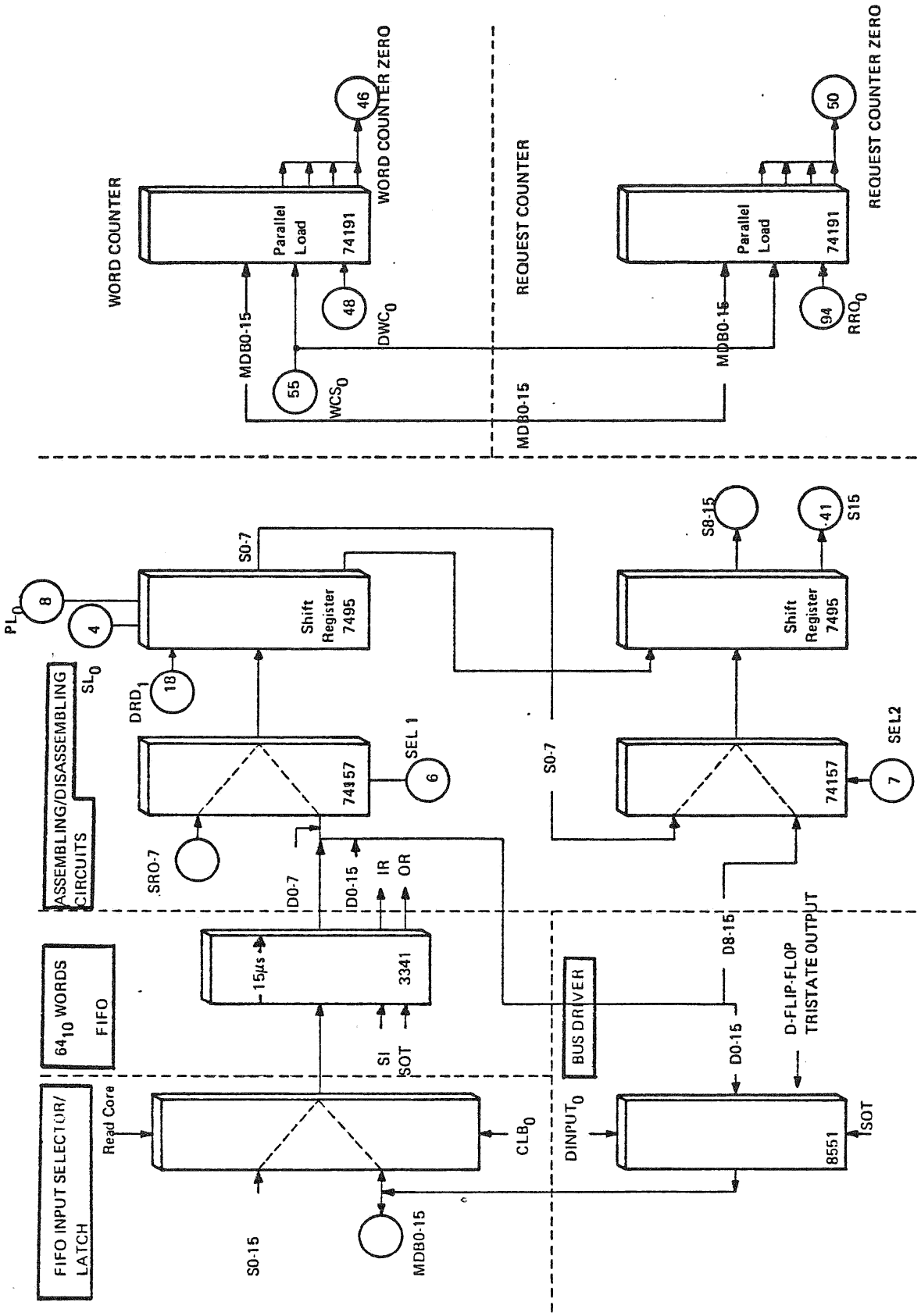


Figure 7.3: 1092 BLOCK DIAGRAM

7.4 *DMA STANDARD MODULES INTERCONNECTION*

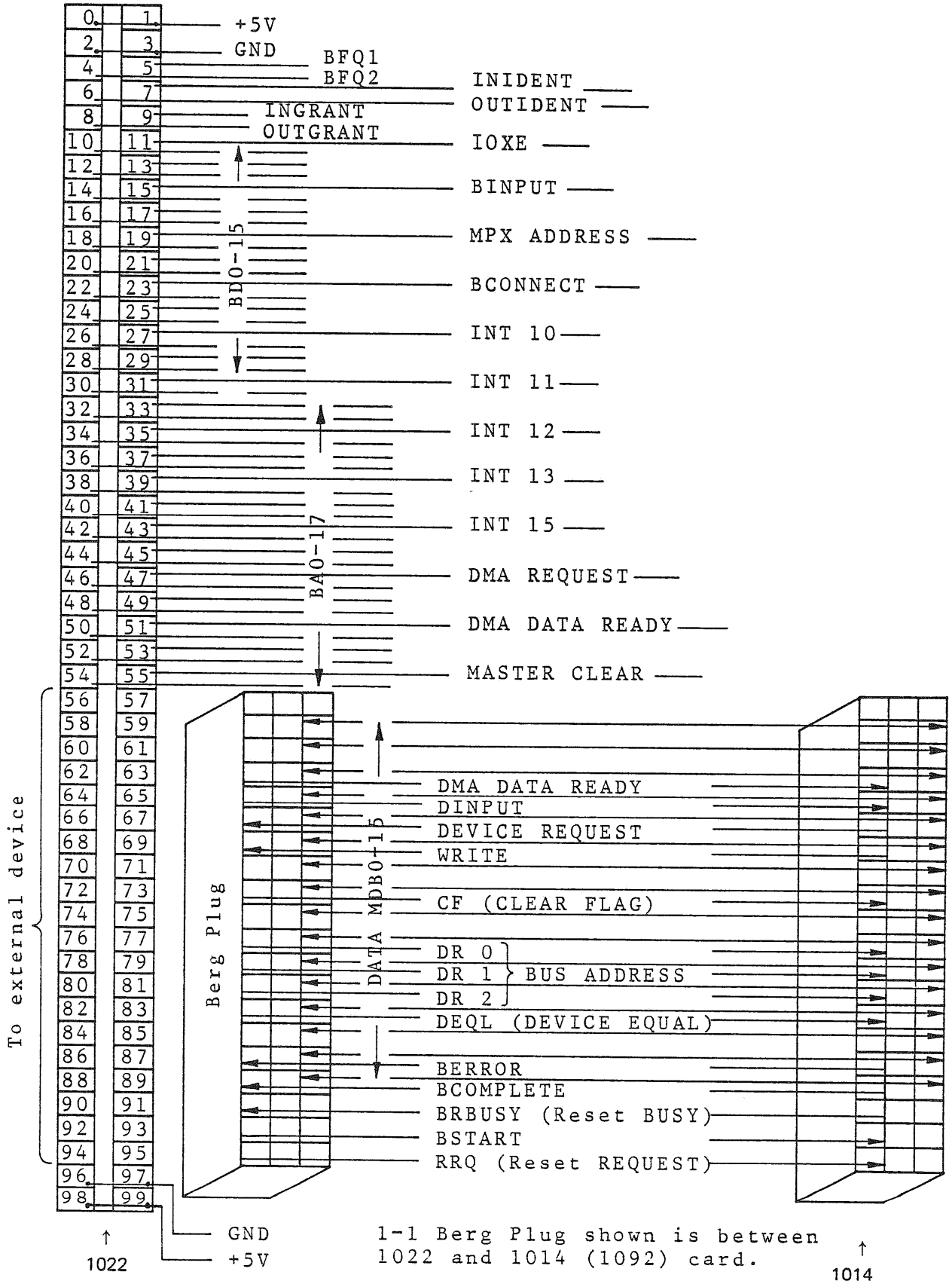


Figure 7.4: SIGNAL DISTRIBUTION I/O BUS B AND C RACK

APPENDIXES

DETAILED CONTENTS

APPENDIX A

SIGNAL DISTRIBUTION WITHIN ONE CARD RACK

	Terminal No.
DATA BIT 0	10
DATA BIT 1	12
DATA BIT 2	13
DATA BIT 3	14
DATA BIT 4	16
DATA BIT 5	17
DATA BIT 6	18
DATA BIT 7	20
DATA BIT 8	21
DATA BIT 9	22
DATA BIT 10	24
DATA BIT 11	25
DATA BIT 12	26
DATA BIT 13	28
DATA BIT 14	29
DATA BIT 15	30
ADDRESS BIT 0	32
ADDRESS BIT 1	33
ADDRESS BIT 2	34
ADDRESS BIT 3	36
ADDRESS BIT 4	37
ADDRESS BIT 5	38
ADDRESS BIT 6	40
ADDRESS BIT 7	41
ADDRESS BIT 8	42
ADDRESS BIT 9	44
ADDRESS BIT 10	45
ADDRESS BIT 11	46
ADDRESS BIT 12	48
ADDRESS BIT 13	49
ADDRESS BIT 14	50
ADDRESS BIT 15	52
ADDRESS BIT 16	53
ADDRESS BIT 17	54
OUTIDENT	6
INIDENT	7
OUTGRANT	8
INGRANT	9
IOXE	11
INPUT	15

	Terminal No.
MPX ADDRESS	19
CONNECT	23
INTERRUPT LEVEL 10	27
INTERRUPT LEVEL 11	31
INTERRUPT LEVEL 12	35
INTERRUPT LEVEL 13	39
INTERRUPT LEVEL 15	43
DMA REQUEST	47
DMA DATA READY	51
MASTER CLEAR	55
DEVICE INTER-CONNECTION	56-95
+5V	0,1,98,99
GROUND	2,3,96,97
BFQ1 19,2 khz	4
BFQ2 307,2 khz	5

APPENDIX B

STANDARD NORD-10 DEVICE NUMBERS AND IDENT CODES

Device No.	*Interrupt Level*	*Ident Code (octal)*	*Device*	*SINTRAN III*
4- 7	13	4	Memory Parity N-12	
10- 13	13	1	Real Time Clock 1	
14- 17	13	2	Real Time Clock 2	
30- 33	12	16	NORD-50/1	
34- 37	10	16	ACM 5	
40- 43	10	15	ACM 1	
44- 47	10	25	ACM 2	
50- 53	10	40	ACM 3	
54- 57	10	41	ACM 4	
60- 77			NORD-50/1 Regs.	
100-107	10-12	4	Synchr. Modem 1	
110-117	10-12	14	Synchr. Modem 2	
120-127	10-12	20	Synchr. Modem 3	
130-137	10-12	24	Synchr. Modem 4	
140-147	10-12	30	Synchr. Modem 5	
150-157	10-12	34	Synchr. Modem 6	
200-207	10-12	60	Asynchr. Modem 1	Terminal 17
210-217	10-12	61	Asynchr. Modem 2	Terminal 18
220-227	10-12	62	Asynchr. Modem 3	Terminal 19
230-237	10-12	63	Asynchr. Modem 4	Terminal 20
240-247	10-12	64	Asynchr. Modem 5	Terminal 21
250-257	10-12	65	Asynchr. Modem 6	Terminal 22
260-267	10-12	66	Asynchr. Modem 7	Terminal 23
270-277	10-12	67	Asynchr. Modem 8	Terminal 24
300-307	10-12	1(120*)	Teletype 1	Terminal 1
310-317	10-12	5(121*)	Teletype 2	Terminal 2
320-327	10-12	6(122*)	Teletype 3	Terminal 3
330-337	10-12	7(123*)	Teletype 4	Terminal 4
340-347	10-12	44	Teletype 5	Terminal 5
350-357	10-12	45	Teletype 6	Terminal 6
360-367	10-12	46	Teletype 7	Terminal 7
370-377	10-12	47	Teletype 8	Terminal 8
400-403	12	2	Paper Tape Reader 1	
404-407	12	22	Paper Tape Reader 2	
410-413	10	2	Paper Tape Punch 1	
414-417	10	22	Paper Tape Punch 2	
420-423	12	3	Card Reader 1	
424-427	12	23	Card Reader 2	
430-433	10	3	Line Printer 1	
434-437	10	23	Line Printer 2	
440-443	10	11	Calcomp Plotter 1	
444-447	10	12	Card Punch 1	
454-457	10	13	Card Punch 2	

* 4 CURRENT-LOOP MODULE 1122

Device No.	*Interrupt Level*	*Ident Code (octal)*	*Device*	*SINTRAN III*
500- 507	11	1	Disk System 1	
510- 517	11	5	Disk System 2	
520- 527	11	3	Magtape Controller 1	
530- 537	11	7	Magtape Controller 2	
540- 547	11	2	Drum 1	
550- 557	11	6	Drum 2	
560- 567	11	12	Drum 3	
570- 577	11	16	Drum 4	
600- 607	11	4	Versatec 1	
610- 617	11	11	Core-to-Core 1	
620- 637	11	10	CDC I/O Link	
640- 647	10-12	124		Terminal 33
650- 657	10-12	125		Terminal 34
660- 667	10-12	126		Terminal 35
670- 677	10-12	127		Terminal 36
700- 707	12	11	CATSY 1	
710- 717	12	21	CATSY 2	
720- 727			A/D Converter	
730- 737	10	10	D/A Converter	
750- 753	13	5	BIG MPM LOG module	
770- 773	12	17	Dig. Reg. 1 Input	
774- 777	10	17	Dig. Reg. 1 Output	
1000-1003	12	26	Dig. Reg. 2 Input	
1004-1007	10	26	Dig. Reg. 2 Output	
1010-1013	12	27	Dig. Reg. 3 Input	
1014-1017	10	27	Dig. Reg. 3 Output	
1020-1023	12	43	Dig. Reg. 4 Input	
1024-1027	10	43	Dig. Reg. 4 Output	
1030-1033	12	116	NORD-50/2	
1034			Watch Dog	
1035			Process Output 1	
1036			Process Output 2	
1037			Process Output 3	
1040-1043	12	15	Process Input 1	
1044-1047	12	25	Process Input 2	
1050-1053	12	40	Process Input 3	
1060-1077			NORD-50/2 Reg.	
1100-1107	10-12	130		Terminal 37
1110-1117	10-12	131		Terminal 38
1120-1127	10-12	132		Terminal 39
1130-1137	10-12	133		Terminal 40
1140-1147	10-12	134		Terminal 41
1150-1157	10-12	135		Terminal 42
1160-1167	10-12	136		Terminal 43
1170-1177	10-12	137		Terminal 44
1200-1207	10-12	70	Asynchr. Modem 9	Terminal 25
1210-1217	10-12	71	Asynchr. Modem 10	Terminal 26
1220-1227	10-12	72	Asynchr. Modem 11	Terminal 27
1230-1237	10-12	73	Asynchr. Modem 12	Terminal 28
1240-1247	10-12	74	Async 13/Photo 1	Terminal 29
1250-1257	10-12	75	Async 14/Photo 2	Terminal 30
1260-1267	10-12	76	Async 15/Photo 3	Terminal 31
1270-1277	10-12	77	Async 16/Photo 4	Terminal 32
1300-1307	10-12	50	Teletype 9	Terminal 9
1310-1317	10-12	51	Teletype 10	Terminal 10
1320-1327	10-12	52	Teletype 11	Terminal 11
1330-1337	10-12	53	Teletype 12	Terminal 12
1340-1347	10-12	54	Teletype 13	Terminal 13
1350-1357	10-12	55	Teletype 14	Terminal 14

Device No.	*Interrupt Level*	*Ident Code (octal)*	*Device*	*SINTRAN III*
1360-1367	10-12	56	Teletype 15	Terminal 15
1370-1377	10-12	57	Teletype 16	Terminal 16
1400-1407	10-12	140		Terminal 45
1410-1417	10-12	141		Terminal 46
1420-1427	10-12	142		Terminal 47
1430-1437	10-12	143		Terminal 48
1500-1507	10-12	144		Terminal 49
1510-1517	10-12	145		Terminal 50
1520-1527	10-12	146		Terminal 51
1530-1537	10-12	147		Terminal 52
1540-1547	11	17	Big Disk System 1	
1550-1557	11	20	Big Disk System 2	
1560-1567	11	21	Floppy Disk 1	
1570-1577	11	22	Floppy Disk 2	
1600-1607	11	14	Versatec 2	
1640-1647	10-12	150		Terminal 53
1650-1657	10-12	151		Terminal 54
1660-1667	10-12	152		Terminal 55
1670-1677	10-12	153		Terminal 56
1700-1707	10-12	154		Terminal 57
1710-1717	10-12	155		Terminal 58
1720-1727	10-12	156		Terminal 59
1730-1737	10-12	157		Terminal 60
1740-1747	10-12	160		Terminal 61
1750-1757	10-12	161		Terminal 62
1760-1767	10-12	162		Terminal 63
1770-1777	10-12	163		Terminal 64

APPENDIX C

TEST LOOPS

1.*Core Address Register (CAR)*

	DRUM:	*HAWK DISK:*	*BIG DISK:*
20/ TRA OPR	150002	150002	150002
IOX CAR	164541	164501	165541
SAA 0	170400	170400	170400
IOX RCAR	164540	164500	165540
COPY SA DX	146157	146157	146157
JMP* -5	124373	124373	124373

X register shall follow the OPR switches

2.*Block Address Test*

20/ SAA 10	170410	170410	170410
IOX CONT	164545	164505	165545
TRA OPR	150002	150002	150002
IOX BAR	164543	164503	165543
SAA 0	170400	170400	170400
IOX RBAR	164546	164506	165546
COPY SA DX	146157	146157	146157
JMP* -7	124371	124371	124371

X register shall follow the OPR switches

3.*Check Ident Code*

20/ SAA 1	170401	170401	170401
IOX LCONT	164545	164505	165545
SAA 0	170400	170400	170400
IDENT PL11	143611	143611	143611
COPY SA DX	146157	146157	146157
JMP* -5	124373	124373	124373

IDENT CODE in X register

C.1 TEST LOOP FOR CDC HAWK DISK INTERFACE

```
10/400                  % CAR (core address
                          register)
12/200                  % WC (word count)
14/  0                  % BAR (block address register). 125252
                          in Test Mode
16/  4                  % CW (control word)

START, 20/044370        % LOAD CAR
       164501           % IOX  CAR
       044370           % LOAD  WC
       164507           % IOX  WC
       044370           % LOAD BAR
       164503           % IOX  BAR
       044370           % LOAD  CW
       164505           % IOX  CW
       164504           % IOX  Read Status
       175025           % BSKIP Active
       124376           % JMP* -2
       175045           % BSKP protect violate
       151013           % WAIT if PROTECT SWITCH is ON
       146157           % Status to X
       124362           % JMP START
```

200 octal words will be read from disk to main memory starting in address 400.

Status register →X register. NB! Parity error in Test Mode.

CAR, BAR, WC and CW can b e changed as desired.

When this "loop" is run in test mode, the test word 125252 and 52525 will be read to consecutive words in memory.

CW	*Real*	*Test*
Read Transfer	4	14
Write transfer	4004	4014
Read parity	10004	10014
Compare test	14004	14014

NB! In test mode, BAR = 125252

C.2 BIG DISK TEST LOOP

```
20/ 044024   START,   LDA CA          % LOAD CORE ADDRESS
    165541            IOX 1541
    044023            LDA BLA
    165543            IOX 1543        % LOAD BLOCK ADDRESS
    044022            LDA WC
    165547            IOX 1547        % LOAD WORD COUNT
    044021            LDA CW
    165545            IOX 1545        % LOAD CONTROL WORD
30/ 165544            IOX 1544        % READ STATUS
    171700            SAX -100
    132400            JNC *0          %   DELAY-INCREMENT   X
                                        AND JUMP IF NEGATIVE
    175235            BSKP ONE 30 DA
    124374            JMP *-4         (Delay due to delay in FIFO)
    146151            COPY SA DD
    165540            IOX 1540        % READ CORE ADDRESS
    064005            SUB CA
40/ 064006            SUB WC
    131002            JAZ *2
    151000            WAIT            % STOP IF ERROR IN CAR
    124355            JMP START
44/ 010000   CA,      10000
    052525   BLA,     52525           % TEST MODE
    001000   WC,      1000
    000014   CW,      14
```

CONTROL WORD (CW) FORMAT:

	Disk Connected (unit 0):	*Test*
Read	4	14
Write	4004	4014
Read parity	10004	10014
Compare	14004	14014
Initiate seek	26004	
Write format	24004	
Seek complete search	30004	
Return to zero seek	34004	

APPENDIX D

PROGRAMMING SPECIFICATION FOR I/O DEVICES

D.1 *NORD-10/S TERMINAL BUFFER (MODULE 1095) PROGRAMMING SPECIFICATION (AS CURRENT-LOOP INTERFACE)*

Terminal Buffer Addresses:

The codes below are relevant for the first terminal. The codes for the first sixteen terminals are found by adding 10_8.N terminal number $(0,1,2.....,17)_8$. For the next sixteen terminals the codes are found by adding $(1000 + 10(N-20))_8$.N= terminal number$(20,11,12,.....,37)_8$. For further information in section 11.

Input Channel (Interrupt Level 12):

Read Data Register

IOX 300

The number of data bits read into the A register is specified by bits 11 and 12 in the input control register. The received character is right justified.

Write Baude-rate Selection

IOX 301

Read Status Register

IOX 302

Write Control Register

IOX 303

Output Channel (Interrupt Level 10):

Write Data Register

IOX 305

The number of bits specified by bits 11 and 12 in the *input* channel control register is written to the output data register, starting with bit 0 and counting upwards.

Read Status Register

IOX 306

Write Control Register

IOX 307

IDENT Code:

The IDENT code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel to level 10. The selection of different ident codes is switch-controlled.

INPUT CHANNEL:

Input Status Register Format:

Bit 0	Ready for transfer interrupt enabled
Bit 1	Not used
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors
Bit 5	Framing error
Bit 6	Parity error
Bit 7	Overrun
Bit 8-10	Not used
Bit 11	Carrier missing
Bit 12	Request to Send missing*
Bit 13	Ready for Sending missing*
Bit 14	Not used
Bit 15	Half duplex*

* Not used when connected to current loop (Used when connected to asynchronous modem).

Notes:

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occurred while working in parity generation/checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Input Control Word Register Format:

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Not used
Bit 2	Active device
Bit 3	Test mode
Bit 4	Device clear
Bits 5-6	Not used
Bit 7	Carriage return delay enable
Bits 8-10	Not used
Bits 11-12	Character length
Bit 13	Number of stop bits
Bit 14	Parity generation/checking
Bit 15	Half duplex*

* When connected to asynchronous modem

Notes:

Bit 2: After a Master Clear or a Device Clear (bit 4), the device has to be activated by writing a 1 into bit 2 of the control register. If not, received data will not be clocked into the receiver data buffer. The control bit will be 1 until 0 is written into it, or it is cleared by Master Clear or Device Clear.

Bit 3: Test mode will loop transmitted data back to received data, and if the other terminal is connected to the line, transmitted data will also be transferred to this terminal.

Bit 4 Gives a clear pulse to the buffer card. After a Device Clear, the buffer card must be initialized.

Bit 7: Carriage return delay enable. If set to 1, this bit will cause a delay of 200-250 milliseconds each time an ASCII carriage return (octal value 15) is transmitted to the terminal. (Useful for Silent 700 terminal with data rate 300 bits/second). Characters with octal values 14, 16 and 17 (form feed, shift out and shift in) will also cause the same delay. (The parity bit is not checked).

Bit 11-
Bit 12: The content of these bits give the following character lengths, both for the input channel and the output channel:

Bit: 12	11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is *added* to the number given in this table.

Bit 13: The number of stop bits will be two if the control bit is 0, and one if the control bit is 1.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

OUTPUT CHANNEL:

Output Status Register Format:

Bit 0	Ready for transfer interrupt enabled
Bit 1	Not used
Bit 2	Device active
Bit 3	Device ready for transfer
Bits 4-10	Not used
Bit 11	Carrier missing*
Bit 12	Request to Send missing*
Bit 13	Ready for Sending missing*
Bit 14	Not used
Bit 15	Half duplex*

* When connected to asynchronous modem

Notes:

Bit 2: This status bit will be a 1 as long as the device is busy transmitting characters.

Bit 3: This bit indicates that the output data buffer is ready to receive a new character. This will be a 1 if bit 2 is 0, but may as well be a 1 when bit 2 is 1 due to the double buffer.

Output-Control Word Register Format:

Bit 0	Enable interrupt on device ready for transfer
Bit 1-15	Not used

Notes:

The device is activated when a character is loaded into the output data-register (IOX 305). There is not need for separate activation.

DATA RATE SELECTION

There are several possibilities to control the data rate for input and output serial data.

The data rate can be selected by:

a) EXTERNAL OSCILLATOR (16 x the bit rate), common for both input and output. The external oscillator is connected to card terminal 81 with a TTL or CCITT - V.24 (EIA RS–232C) signal level.

In this case a high signal has to be connected to terminal 80 (select external oscillator). Switches as for 9600 baud.

b) SWITCH SETTING on card. Independent speed for input and output. The switch in position 9 B 6 must be in the ON position, and the switch setting is sensed each time Master Clear is pressed. The selectable baud rates are: 9600, 4800, 2400, 1200, 600, 300, 200, 150, 110, 100, 75 and 50. In this case, no high signal must be connected to terminal 81. A high signal to terminal 80 will stop both input and output as long as the signal is high (BUSY).

Switch settings for the different baud rates are given in Table 1.

c) IOX INSTRUCTION. The baud rate selection by software corresponds much to the switch setting referred to under b.

Input and output are independent, and are selected by the same IOX instruction (Group device number + 1). The content of the A register before the IOX instruction is executed determines the baud rate. The 4 least significant bits (0-3) are used for the input channel, and the next 4 (bits 4-7) are used for the output channel. Table 1 gives the bit pattern and corresponding baud rate.

The BUSY signal (terminal 80) will, as mentioned under b), stop the feeding of input and output data.

If the switch in position 9 B 6 is ON, pressing of the Master Clear button will select the baud rate given by the switches (15E1-15E8). If the switch in position 9 B 6 is OFF, the baud rate setting is only due to the IOX instruction, and is not changed by pressing Master Clear.

Note: A programmed device clear has no influence on the baud rate setting, but must always be given after the baud rate has been changed.

INPUT CHANNEL (TO THE COMPUTER):

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REGISTER								
	15E4	15E3	15E2	15E1	Bit 7							Bit 0	Octal
9600	ON	ON	ON	ON	X	X	X	X	0	0	0	0	0
4800	ON	ON	ON	OFF	X	X	X	X	0	0	0	1	1
2400	ON	ON	ON	OFF	X	X	X	X	0	0	1	0	2
1200	ON	ON	OFF	OFF	X	X	X	X	0	0	1	1	3
600	OFF	ON	ON	ON	X	X	X	X	1	0	0	0	10
300	OFF	ON	ON	OFF	X	X	X	X	1	0	0	1	11
200	OFF	OFF	ON	OFF	X	X	X	X	1	1	0	1	15
150	OFF	ON	OFF	ON	X	X	X	X	1	0	1	0	12
110	OFF	OFF	ON	ON	X	X	X	X	1	1	0	0	14
100	OFF	OFF	OFF	ON	X	X	X	X	1	1	1	0	16
75	OFF	ON	OFF	OFF	X	X	X	X	1	0	1	1	13
50	OFF	OFF	OFF	OFF	X	X	X	X	1	1	1	1	17

OUTPUT CHANNEL (FROM THE COMPUTER):

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REGISTER								
	15E8	15E7	15E6	15E5	Bit 7							Bit 0	Octal
9600	ON	ON	ON	ON	0	0	0	0	X	X	X	X	000
4800	ON	ON	ON	OFF	0	0	0	1	X	X	X	X	020
2400	ON	ON	OFF	ON	0	0	1	0	X	X	X	X	040
1200	ON	ON	OFF	OFF	0	0	1	1	X	X	X	X	060
600	OFF	ON	ON	ON	1	0	0	0	X	X	X	X	200
300	OFF	ON	ON	OFF	1	0	0	1	X	X	X	X	220
200	OFF	OFF	ON	OFF	1	1	0	1	X	X	X	X	320
150	OFF	ON	OFF	ON	1	0	1	0	X	X	X	X	240
110	OFF	OFF	ON	ON	1	1	0	0	X	X	X	X	300
100	OFF	OFF	OFF	ON	1	1	1	0	X	X	X	X	340
75	OFF	ON	OFF	OFF	1	0	1	1	X	X	X	X	260
50	OFF	OFF	OFF	OFF	1	1	1	1	X	X	X	X	360

Note:
Input and output baud rates are selected by the same IOX instruction. If the A register is set to octal value 14 before the IOX instruction is executed, 110 baud will be selected for input, and 9600 baud will be selected for output. To get 110 baud on both the input and output channel, the octal value 314 should be placed in the A register before the IOX instruction is executed.

IDENT CODES AND INTERRUPT MECHNAISM

Ident Codes

The ident codes are binary coded by the switches in position 1E, with 0 corresponding to ON and 1 corresponding to OFF.

EXAMPLES:

Ident code	1E7	1E6	1E5	1E4	1E3	1E2	1E1
0_8	ON	ON	ON	ON	ON	ON	ON
1_8	ON	ON	ON	ON	ON	ON	OFF
2_8	ON	ON	ON	ON	ON	OFF	ON
60_8	ON	OFF	OFF	ON	ON	ON	ON
77_8	ON	OFF	OFF	OFF	OFF	OFF	OFF
155_8	OFF	OFF	ON	OFF	OFF	ON	OFF

All ident codes from 0 to 177_8 can be selected.

Interrupt Mechanism

What is needed for a device to give an interrupt?

First of all the device must be ready for a transfer, i.e. status bit 3 must be on. For input this means that a whole character is received by the input buffer, and is ready to be read into the A register. For output it means that it is possible to place at least one more character in the output buffer. Secondly, interrupt on ready for transfer must be enabled. It means that a 1 is written into the control register bit 0 (which also is status register bit 0). The AND function of Ready for Transfer and Ready for Transfer Interrupt Enabled is gated to "wire-or" lines, separate for input and output. Input is connected to interrupt level 12 (terminal 35) and output is connected to interrupt level 10 (terminal 27).

When an interrupt is detected (dependent on the status in CPU and the program), the CPU usually responds by executing an IDENT instruction for the interrupting level. The level shift and interrupt mechanism in the CPU will not be described here. What is usually seen on the card is that sooner or later the INIDENT signal (terminal 7) will occur with the correct level code (determined by Bus Address bits 0 and 1 (terminals 32 and 33). The timing here is that the Bus Address bits occur before signal occurs. Now, one part of the schotky data selector/multiplexer (74S157) in position 13A is used as a latch, freezing the status of the INT signal at the moment INIDENT occurs. If it is a 1, TINT will be a 1. This in turn results in INPUT and CONNECT back to the CPU, and the interrupt enable flip-flolp for the selected level is cleared by CLINT (13A7) gated through the 74157 circuit in position 11A. (11A4 or 11A7). As the interrupt flag is AND function of the enable flip-flop and the Ready for Transfer status, the flag is cleared when the enable flip-flop is cleared.

Together with CONNECT and INPUT back to the CPU, the Ident Code is gated to the Data Bus (DB 0-7).

The ident code is identical for input and output channel.

D.2 *SPECIFICATION OF TAPE READER INTERFACE*

Standard device number 0400 $(0400\text{-}0403)_8$
Number of device number 4
Standard interrupt level 12_{10}
Standard ident number 2

Control Word IOX Device Number +3:

Bit 0	Enable interrupt on ready for transfer
Bit 1	Not used
Bit 2	Activate device (start reading next character on tape)
Bit 3	Test
Bit 4	Device clear
Bits 5-15	Not used

Status Word IOX Device Number +2:

Bit 0	Interrupt enabled on ready for transfer
Bit 2	Read active
Bit 3	Reader ready for transfer (character read)

IOX device no. +1 Not used

Data Read IOX Device Number + 0:

Read character. The same character may be read several times if desired.

TEST:

When bit 3 in the control word is set to 1, the interface may be tested without reader.

If bit 2 is also set to 1, the interface will give "ready for transfer" after a while.

If "ready for transfer" is constantly 1, the data register will increment for each time IOX device no. + 3 (control word write) is used, and then it is possible to test the data patch.

D.3 *SPECIFICATION OF THE PAPER TAPE PUNCH INTERFACE*

Standard device number 0410 $(0410\text{-}0413)_8$
Number of device number 4
Standard interrupt level 10_{10}
Standard ident no. 2

Write Control Word IOX Device Number +3:

Bit 0	Enable interrupt
Bit 1	Not used
Bit 2	Activate device (punch character now in buffer)
Bit 3	Test
Bit 4	Device clear
Bits 5-15	Not used

Read Status Word IOX Device Number +2:

Bit 0	Interrupt enabled
Bit 2	Device activate
Bit 3	Device ready

Write data word IOX Device no. + 1.

Write the 8 A-register bits to be punched in a buffer register.

Read data IOX Device number + 0:

Only used under test.

It is not wise to write a character into the buffer if the punch is not ready.

TEST:

The interface may be tested without punch.

When bit 3 in the control word is one, the buffer register may be read back by IOX device number. If the interface is activated, it will become "ready for transfer" after a while.

D.4 *SPECIFICATIONS OF LINE PRINTER INTERFACE FOR CDC 9380*

Standard device number 0430 $(0430\text{-}0433)_8$.
Number of device number 4.
Standard interrupt level 10_{10}.
Standard ident number 3.

Write Control Word IOX Device Number + 3:

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate device (print character now in buffer)
Bit 3	Test
Bit 4	Device and interface clear
Bit 5-15	Not used

Read Status Word IOX Device Number + 2:

Bit 0	Interrupt enabled on ready
Bit 1	Interrupt enabled on error
Bit 2	Not used
Bit 3	Ready for transfer
Bit 4	Error, bit 5 or 6 set
Bit 5	Line printer not ready
Bit 6	Out of paper
Bit 7	Compressed pitch
Bit 8	LP9 is on, to indicate to the controller that data on the lines is format information and is interpreted as control code
Bit 9	Inhibit, illegal character in buffer
Bit 10	Not used
Bit 11	Band detect
Bit 12	Band detect

Bit 11	Bit 12	Type of band
0	0	128 characters
1	0	96 characters
0	1	64 characters
1	1	48 characters

Note! This interface is only handling 64, 96 character printers.

Bit 13-15 Not used

Write Data Word IOX DEV NO + 1

Writes a character in the buffer register.

All character codes $0\text{-}37_8$ are illegal and ignored by the interface, except following control codes:

11_8 : HT (Gives space in CDC controller)

12_8 : LF

14_8 : FF

15_8 : CR

$20_8 - 33_8$ VFU channels give LP9 and disable LP5

20_8 VFU channel 1 (FF)
21_8 VFU channel 2
|
|
|
33_8 VFU channel 12

Read Data Word IOX DEV NO

It is possible to read back the data written in the buffer register when running in test mode (bit 3 set in control word).

D.5 *SPECIFICATION OF CARD READER INTERFACE (DOCUMENTATION) FOR NORD-10/S*

Standard device number 0420 $(0420\text{-}0423)_8$.
Number of device number 4.
Interrupt level 12_{10}.
Ident number 3.

Write Control Word IOX Device + 3:

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate.): Feed one card. Clear end of card.
Bit 3	Test
Bit 4	Device clear. Clear interrupt flip-flop, overrun flip-flop. Continue feed flip-flop and set end of card.
Bit 5-8	Not used
Bit 9	Continuous feed): feed next card immediately.
Bit 10-15	Not used

Read Status Word IOX Device + 2:

Bit 0	Interrupt enabled on ready for transfer
Bit 1	Interrupt enabled on error
Bit 2	Card reader active. Signal from card reader.
Bit 3	Ready for transfer): a column may be read. This bit is turned off by "read data" IOX DEV.
Bit 4	Bits 5-9 set, error.
Bit 5	Hopper check error set from card reader.
Bit 6	Light or dark error from card reader.
Bit 7	Motion check error from card reader.
Bit 8	Overrun, one column was lost because it was not read before the next column was strobed into buffer. Cleared by MASTER CLEAR.
Bit 9	End of card.
Bits 10-15	

Be aware that the card reader sends hopper check while reading the last card.

Write Data IOX Device + 1:

Only used for testing the interface without card reader.

Read Data IOX Device:

Read last column.

TEST:

The interface may be tested without card reader. When bit 3 in the control word is set to one, the interface is in "test mode".

An IOX Device + 1 will simulate a column ready by the interface, set ready for transfer and increment the data register.

An "end of card" is simulated by IOX Device + 1 and bit 5 is set to one.

D.6 *NORD-10/S CDC HAWK DISK PROGRAMMING SPECIFICATIONS*

Disk Device Register Address:

The codes below are relevant for disk system 1. Each disk system may consist of 4 units. For disk system 2 add 10_8 to the specified codes.

Read Core Address

IOX 500

Load Core Address

IOX 501

Read Sector Counter

IOX 502

Load Block Address

IOX 503

Read Status Register

IOX 504

Load Control Word

IOX 505

Seek Instruction

IOX 506

Load Word Count Register

IOX 507

The minimum number of words to be transferred is one sector, i.e., 200_8 words, the maximum number of words is one track, i.e., 24 sectors (6000_8 words).

Read Block Address

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (test mode), the instruction

IOX 506

will return the previously loaded block address to the A register.

Control Word

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Enable interrupt on errors
Bit 2	Activate device
Bit 3	Test mode
Bit 4	Device clear
Bit 5	Address bit 16
Bit 6	Address bit 17
Bit 7-8	Not assigned
Bit 9	Unit select
Bit 10	Unit select
Bit 11	Device operation
Bit 12	Device operation
Bit 13	Marginal Recovery
Bit 14	Not assigned
Bit 15	Write format

Unit Select Code:

Bit 10	9	
0	0	Unit 0
0	1	Unit 1
1	0	Unit 2
1	1	Unit 3

Device Operation Code:

Bit 12	11	
0	0	Read transfer
0	1	Write transfer
1	0	Read parity
1	1	Compare

To format a disk, the switch for formatting has to be turned on, Write Transfer, and Write Format must be specified.

Status Word

Bit 0	Ready for transfer, interrupt enabled
Bit 1	Error interrupt enabled
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors (status bits 5-11)
Bit 5	Write protect violate
Bit 6	Time out
Bit 7	Hardware error
Bit 8	Address mismatch
Bit 9	Parity error
Bit 10	Compare error
Bit 11	Missing clock error
Bit 12	Transfer complete
Bit 13	Transfer on
Bit 14	On cylinder
Bit 15	Bit 15 loaded by previous control word

Interrupt

The disk interrupt level is 11 and the ident number for the first disk system is 1 .

D.7 *NORD-10/S BIG-DISK PROGRAMMING SPECIFICATION (33 or 66M BYTE)*

DISK DEVICE REGISTER ADDRESS

The codes below are relevant for disk system I. Each disk system may consist of 8 disk units. For disk system II add 10_8 to the specified codes.

Read Core Address

IOX 1540

Load Core Address

IOX 1541

Read Seek Condition

IOX 1542

Load Block Address

IOX 1543

Read Status Register

IOX 1544

Load Control Word

IOX 1545

Load Word Count Register

IOX 1547

The maximum number of words to be transferred are 16 sectors, 8K words.

Read Block Address

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (Test mode) the instruction

IOX 1546

will return the previous loaded block address to the A-register.

DISK FORMAT

Disk Address

The 16 bit in the Block Address Register have the following meaning:

Bit	
0-3	Sector number, 16 sectors per track (512_8 words pr. sector)
4-6	Surface number, 5 surfaces
7-15	Cylinder number, totally 411 cylinders (0-410)

The most significant bit (bit 15) in the Control word is used to extend the cylinder address to 10 bits, thus enabling a cylinder address of maximum 822 cylinders. This is only relevant for 66 Mbyte disks.

CONTROL WORD

Control Word Content

Bit	
0	Enable interrupt on device ready for transfer
1	Enable interrupt on errors
2	Activate device operation
3	Test mode/Select unit
4	Device clear (clear the activate flip-flop) and controller error bits
5	Address bit 16
6	Address bit 17
7-9	Unit select (maximum 8 units)
10	Marginal recovery cycle
11-14	Device operation code
15	Extended cylinder address

Select Unit

When a Control Word is loaded the disk unit number (0-7) has to be set up in bits 7-9. If the transfer is changed from one unit to another, the new unit must be selected with a special program sequence. Bit 3 in the Control Word, select unit bit (test bit) is used.

Example, selects unit one:

```
UNIT,       200                  %  Unit one, one in bit 7-9
SE LUNIT,   LDA  UNIT            %  Load unit number
            AAA  10              %  Set select unit bit, bit 3
            IOX  1545            %  Load Control Word
            SAA  20              %  Device clear to
            IOX  LCW             %  Clear possible error status
            IOX  1544            %  Read status
            BSKP IF ZERO 150 DA  %  Test if unit ready
            JMP  ERROR           %  No unit ready
                                 %  Continue
```

Marginal Recovery Cycle

The marginal recovery cycle (control word bit 10) may be used in connection with read operation codes M0, M2 and M3 as defined in the following section. This control bit is included to be an aid in recovering marginal data. For consecutive read transfers with this bit set, the controller will cycle through the following conditions:

1	Marginal read	: Servo offset positive, data strobe early
2	Marginal read	: No servo offset, data strobe early
3	Marginal read	: Servo offset negative, data strobe early
4	Marginal read	: Servo offset positive, nominal data strobe
5	Marginal read	: Servo offset negative, nominal data strobe
6	Marginal read	: Servo offset positive, data strobe late
7	Marginal read	: No servo offset, data strobe late
8	Marginal read	: Servo offset negative, data strobe late
9 = 1	etc.	

Device Operation

All device operation codes will be activated when the code is given together with bit 3 (activate device). For all codes except M6, the correct unit number must also be selected.

Bit	14	13	12	11		
	0	0	0	0	MO	Read transfer
	0	0	0	1	M1	Write transfer
	0	0	1	0	M2	Read parity transfer
	0	0	1	1	M3	Compare transfer
	0	1	0	0	M4	Initiate seek
	0	1	0	1	M5	Write format
	0	1	1	0	M6	Seek complete search
	0	1	1	1	M7	Return to zero seek

MO *Read transfer:*

This operation causes the controller to transfer data from the disk to the computer memory. The number of blocks transferred depends upon the word count as defined by the Word Count Register.

M1 *Write transfer:*

Transfer of data from the computer memory to the disk.

M2 *Read parity transfer:*

The controller will check the parity on the address and data of the sectors specified. Data is transferred to the controller and the cyclic check word for both the address field and the data field of a sector is compared with the correct check word as generated by the controller. No data transfer to the computer memory is performed.

M3 *Compare transfer:*

This function is included to positively check the data written on the disk. During compare transfer the controller compared the data read from the disk and data from the computer memory is compared bit by bit. Mismatch causes compare error bit to be set.

M4 *Initiate seek:*

This function is included to enable a unit to position the heads prior to a data transfer. The heads will be positioned according to the content of the Block Address Register. As soon as this function is accepted by the disk, the operation will be completed.

M5 *Write format:*

Together with a switch on a card in the interface set, this function will cause the controller to write the address field within each sector.

M6 *Seek complete search:*

This function will enable the controller to go in a waiting state until any unit has completed a seek. This function is independent of the unit select code in the control word.

M7 *Return to zero seek:*

This will cause the selected disk to perform a seek to cylinder 0 and will also clear the seek error bit in the unit.

Extended Cylinder Address:

Bit 15 in the control word is used as an extension to the cylinder address in the Block Address Register. This extended bit is used to allow addresses of up to 822 cylinders.

READ SEEK CONDITION (IOX 1542)

Bit 0-7 SEEK COMPLETE

Seek complete status for unit 0-7. True if the unit has moved the heads to the correct cylinder or a seek error has occurred, and the heads are under the sector number prior to the one specified by the block address loaded before the initiate seek command. The seek complete status will only be set if an initiate seek command for that unit has first been issued.

Thus, after an initiate seek command is given, the SEEK COMPLETE bit for that unit will appear once per revolution after the unit is positioned on the correct cylinder, or a seek error has occurred. The condition will last until a transfer command is given.

Bit 8-10 UNIT SELECT

The unit number as loaded by the last control word.

Bit 11 SEEK ERROR

Seek error for that selected unit. This signal indicates that the unit was unable to complete a move within 500 ms, or that the heads have moved to a position outside the recording field, or that an address greater than the maximum number of tracks has been selected.

This signal will only be cleared by performing a RETURN to ZERO command on that unit.

READ STATUS

Status word:

Bit 0	Ready for transfer interrupt enabled.
Bit 1	Error interrupt enabled.
Bit 2	Controller active.
Bit 3	Controller finished with a device operation
Bit 4	Inclusive or of errors (Bit 5-13).
Bit 5	Illegal load i.e. load while status bit 2 is true, or load of block address while the unit is not on cylinder.
Bit 6	Time out
Bit 7	Hardware error (Disk fault + missing read clocks + missing servo clocks).
Bit 8	Address mismatch
Bit 9	Parity error
Bit 10	Compare error
Bit 11	DMA channel error
Bit 12	Abnormal completion
Bit 13	Disk unit not ready
Bit 14	On cylinder
Bit 15	Extended cylinder address

INTERRUPT

The disk interrupt level is 11 and the ident number for disk system I is 17 and for disk system II 20.

D.8 *PROGRAM SPECIFICATIONS FOR PERTEC 8000 and 9000 MAG-TAPE*

Device no. and registers.

Device no. is 520-527 for first system.

Register:	IOX
Read Core Address	520
Load Core Address	521
Read Modus	522
Load Modus	523
Read Status	524
Load Control	525
In Test, Read previous loaded Modus (523)	526
Load Word Count	527
Interrupt Level	11

[Statement in sharp parantheses is eqivalent meaning on Tandberg].

Load Control Word (IOX 525)

Bit	
0	Enable interrupt on device ready for transfer
1	Enable interrupt on errors
2	Activate
3	Test mode
4	Device clear
5	Address bit 16
6	Address bit 17
7-10	Not used
11-12	Device operation code
13-14	These bits must be zero
15	On the fly operation, interrupt when tape-unit is deaccelerating

12-11

0 0	A normal operation given by the modus-code.
0 1	Not used
1 0	Rewind
1 1	Off line [Tandberg Rewind and unload]

Read Status (IOX 524)

Bit	
0	The ready interrupt enabled
1	Error interrupt enabled
2	Device active
3	Device ready for transfer
4	Error, inclusive OR of bit 5-12
5	Control or modus word error. Trying to write on protected tape, tape unit not on-line, etc.
6	Bad data block
7	Tape mark detected
8	Not usable
9	End of tape detected
10	Word counter not zero
11	DMA-error
12	Overflow in read
13	Formatter busy [Tape busy]
14	Data busy [Formatter busy]
15	Bit 15 loaded by previous control word. On the fly operation, interrupt when bit 14 goes off.

Load Modus (IOX 523)

Bit 0-8 a modus code

Bit		
0	Not used [556 BPI]	
1	Not used [220 BPI]	
2	Reverse	
3	Write	
4	Space/Erase	
5	File mark	
6	Edit	[High speed]
7	Parity (7 tr.)	[Parity 7 tr.] (even parity)
8	THR2	[Threshold]

Bits 2-5 are combined to give an operation

2	3	4	5	
0	0	0	0	Read forward
1	0	0	0	Read reverse
0	1	0	0	Write
0	0	1	0	Space forward
1	0	1	0	Space reverse
0	1	1	0	Erase
0	1	0	1	Write file mark
0	0	1	1	Search for file mark
1	0	1	1	Search reverse for file mark

Other combinations are not standard

Bit 6 Edit is used to overwrite one record between others.

Bit	
9-11	Not used
12-13	Tape unit no. (1 of 4) [One of 8 units on Tandberg]
14	Formatter no. (1 of 2) [One of 8 units on Tandberg]
15	Read odd no. of characters

Note: Odd no. of characters Modus 15 should not be used together with on-the-fly operation (control bit 15).

Read Modus (IOX 522)

Bit	
0	Online
1	Write enable ring present
2	Tape standing on load point
3	Hard error [CRC]
4	Corrected error [LRC]
5- 8	Undefined [no. of VRC]
9-15	Undefined

APPENDIX E

E.1 *MODEL 33 ASR/KSR TELETYPE CODE (ASC II) IN BINARY FORM*

HOLE PUNCHED = MARK = 1
NO HOLE PUNCHED = SPACE = 0

Most significant bit
Least significant bit
7 6 5 4 3 2 1 0

@	SPACE	NULL/IDLE			0	0	0	0	0
A	!	START OF MESSAGE			0	0	0	0	1
B	"	END OF ADDRESS			0	0	0	1	0
C	#	END OF MESSAGE			0	0	0	1	1
D	$	END OF TRANSMISSION			0	0	1	0	0
E	%	WHO ARE YOU			0	0	1	0	1
F	&	ARE YOU			0	0	1	1	0
G	'	BELL			0	0	1	1	1
H	(	FORMAT EFFECTOR			0	1	0	0	0
I	)	HORIZONTAL TAB			0	1	0	0	1
J	*	LINE FEED			0	1	0	1	0
K	+	VERTICAL TAB			0	1	0	1	1
L	,	FORM FEED			0	1	1	0	0
M	–	CARRIAGE RETURN			0	1	1	0	1
N	.	SHIFT OUT			0	1	1	1	0
O	/	SHIFT IN			0	1	1	1	1
P	0	DCO			1	0	0	0	0
Q	1	READER ON			1	0	0	0	1
R	2	TAPE (AUX ON)			1	0	0	1	0
S	3	READER OFF			1	0	0	1	1
T	4	(AUX OFF)			1	0	1	0	0
U	5	ERROR			1	0	1	0	1
V	6	SYNCHRONOUS IDLE			1	0	1	1	0
W	7	LOGICAL END OF MEDIA			1	0	1	1	1
X	8	S 0			1	1	0	0	0
Y	9	S 1			1	1	0	0	1
Z	:	S 2			1	1	0	1	0
[	;	S 3			1	1	0	1	1
\	<	S 4			1	1	1	0	0
]	=	S 5			1	1	1	0	1
↑	>	S 6			1	1	1	1	0
←	?	S 7			1	1	1	1	1

0 0	Same
0 1	Same
1 0	Same
1 1	Same

RUB OUT

PARITY

APPENDIX F

CARD MODULES

F.1 *GENERAL*

Dimensions of card modules installed in NORD 10, NORD 10S, NORD 12, NORD 42 and NORD 50 designed before summer 1977 are given in Figure 1.

Dimensions of modules designed after summer 1977 are given in Figure 3.

F.2 *COORDINATE SYSTEMS*

To identify positions on the cards, two different coordinate systems are used, one to identify plated-through holes, and the other to identify component positions on the card.

F.2.1 *THROUGH-PLATING COORDINATES*

On Figure 1, the system used to identify through-platings is shown. Every hole except those close to the finger contacts is identified by a capital letter (A to V) and a number (1 to 53). The coordinates for the marked through-plating near the centre of the card is *K30*. The through-platings close to the finger contacts are identified by the corresponding finger contact number terminal on component side. It is written as a colon and an even number (0 to 98).

F.2.2 *COMPONENT COORDINATES*

The coordinate system used for components is mainly for integrated circuits. These coordinates are written as a row number from 1 to 19 and then a letter for the column. Some of these numbers are printed on the card, and are partly shown in Figure 1. 1 is the row between plated-through holes A and B, 2 is the row between plated-through holes B anc C, and so on. The letters, however, are not fixed to physical dimensions on the card, but are dependent on where on the card the integrated circuits are placed. The rules are that all integrated circuits in the column close to the finger contacts are column A. The next one B and so on. With normal size on the integrated circuits it is possible to use the letters from A to (and including) the letter F*. IC's with 24 and 40 pins may cover for instance 3 and 4, B and C. The notation in this case is *3B*. (Figure 2).

*G for the later modules.

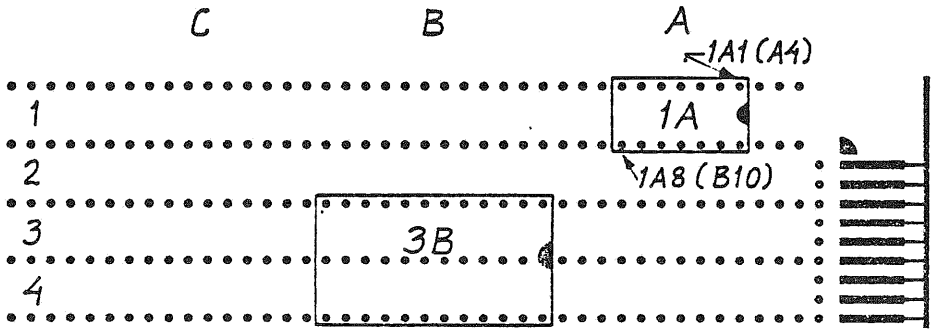


Figure 2: IC COORDINATES

The components coordinates are often used with an additional number to identify pin on the IC. In figure 1 the IC pin 1A1 is located in through-plating A4, and 1A8 is located in through-plating B10.

F.3 *CARD MODULES POWER-CONNECTION*

Voltage:	*Finger-contact:*
+5V	0,1,98,99
GROUND (+5V)	2,3,96,97
−5V	58,59
GROUND (−5V)	56,57
−12V	62,63
GROUND (−12V)	60,61
+12V	66,67
GROUND (+12V)	64,65
+24V	70,71
GROUND (+24V)	68,69

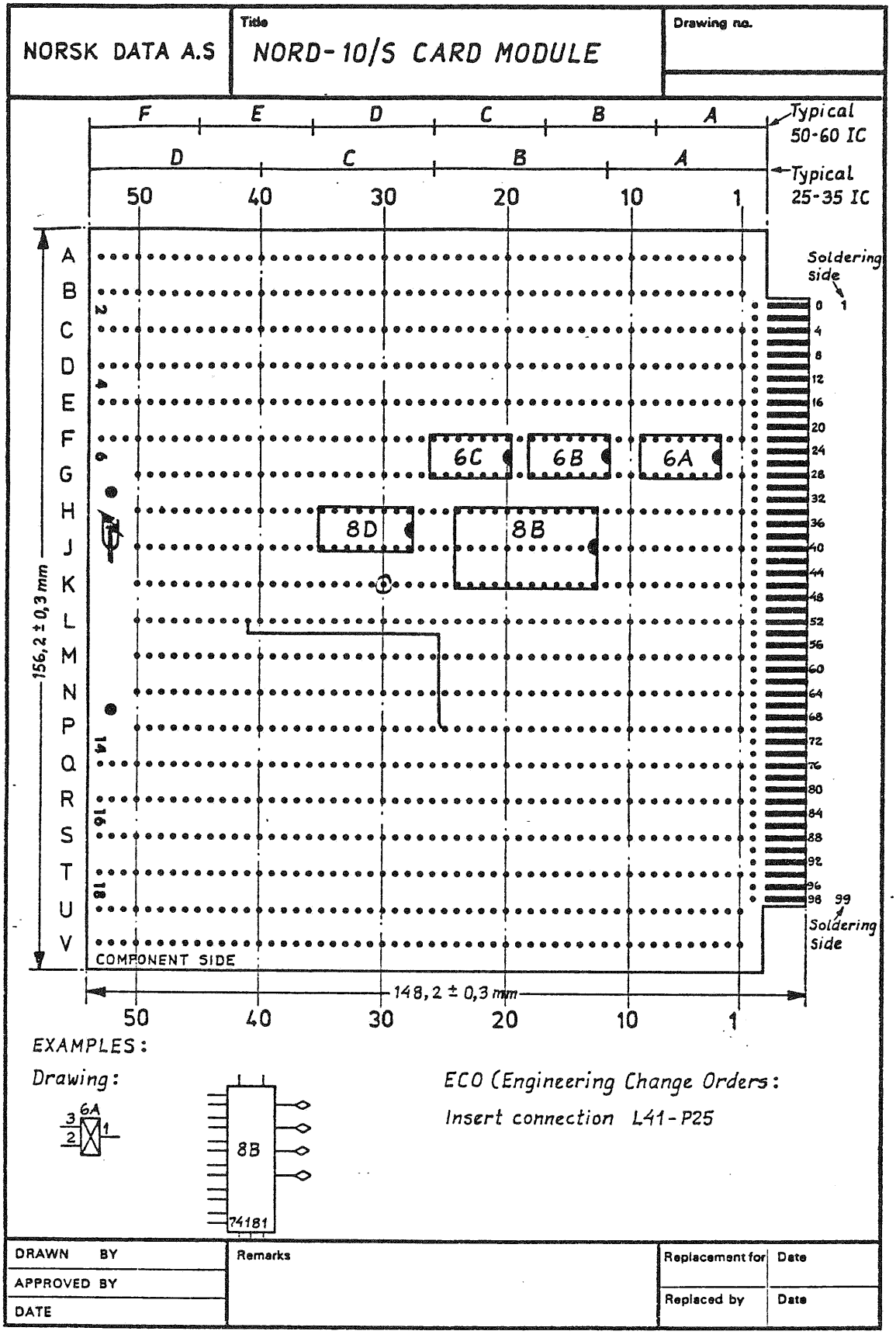
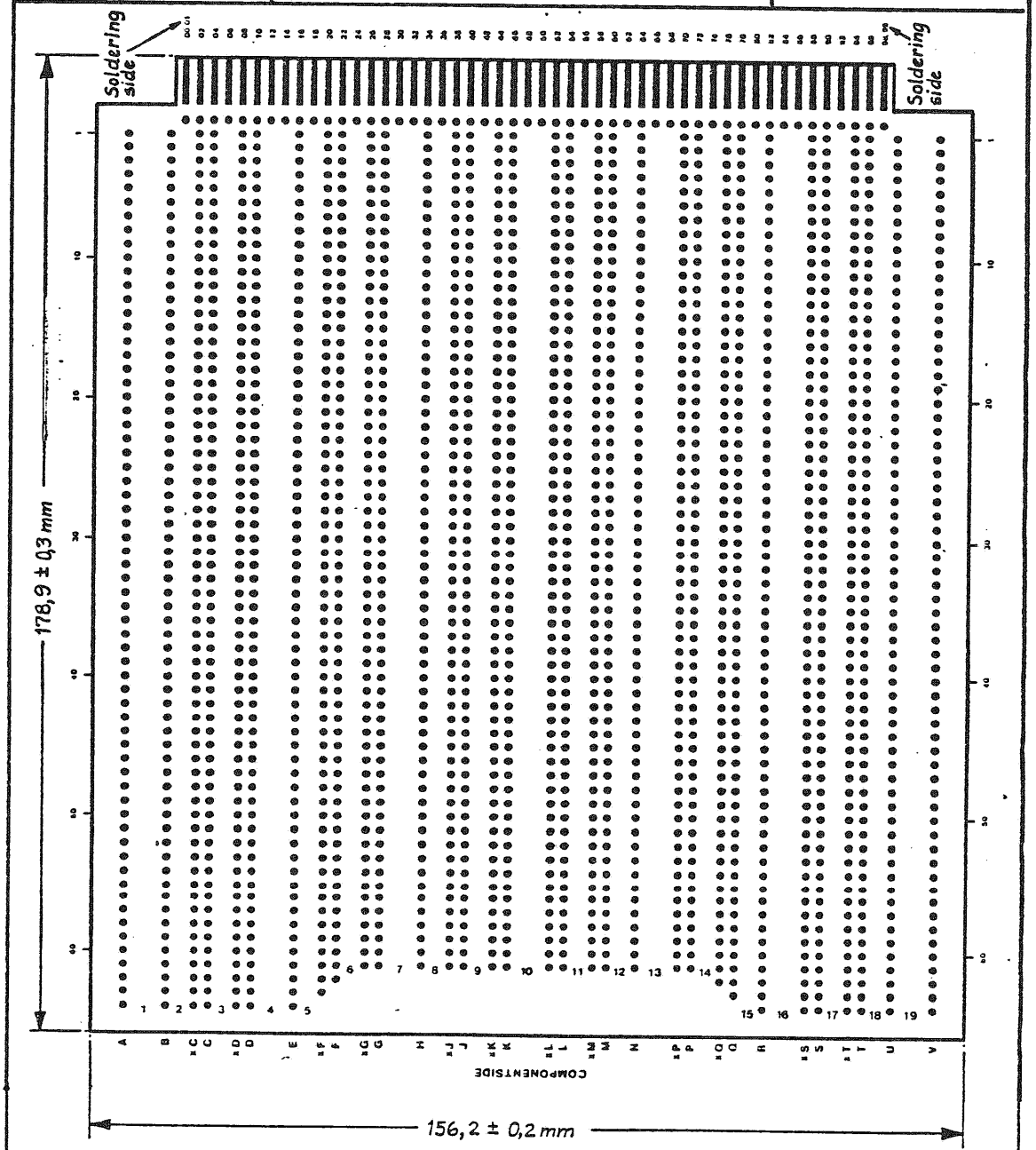

NORSK DATA A.S
Title
NORD-10/S CARD MODULE
Drawing no.
F E D C B A
D C B A
Typical 50-60 IC
Typical 25-35 IC
50 40 30 20 10 1
A B C D E F G H J K L M N P Q R S T U V
2 4 6 14 16 18
6C 6B 6A
8D 8B
Soldering side
0 1 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88 92 96 98 99
Soldering Side
156,2 ± 0,3 mm
148,2 ± 0,3 mm
COMPONENT SIDE
EXAMPLES:
Drawing:
6A
3
2
1
8B
74181
ECO (Engineering Change Orders:
Insert connection L41-P25
DRAWN BY
APPROVED BY
DATE
Remarks
Replacement for
Date
Replaced by
Date

FIGURE 1

NORSK DATA A.S	Title: NORD-10/S CARD MODULE	Drawing no.



DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

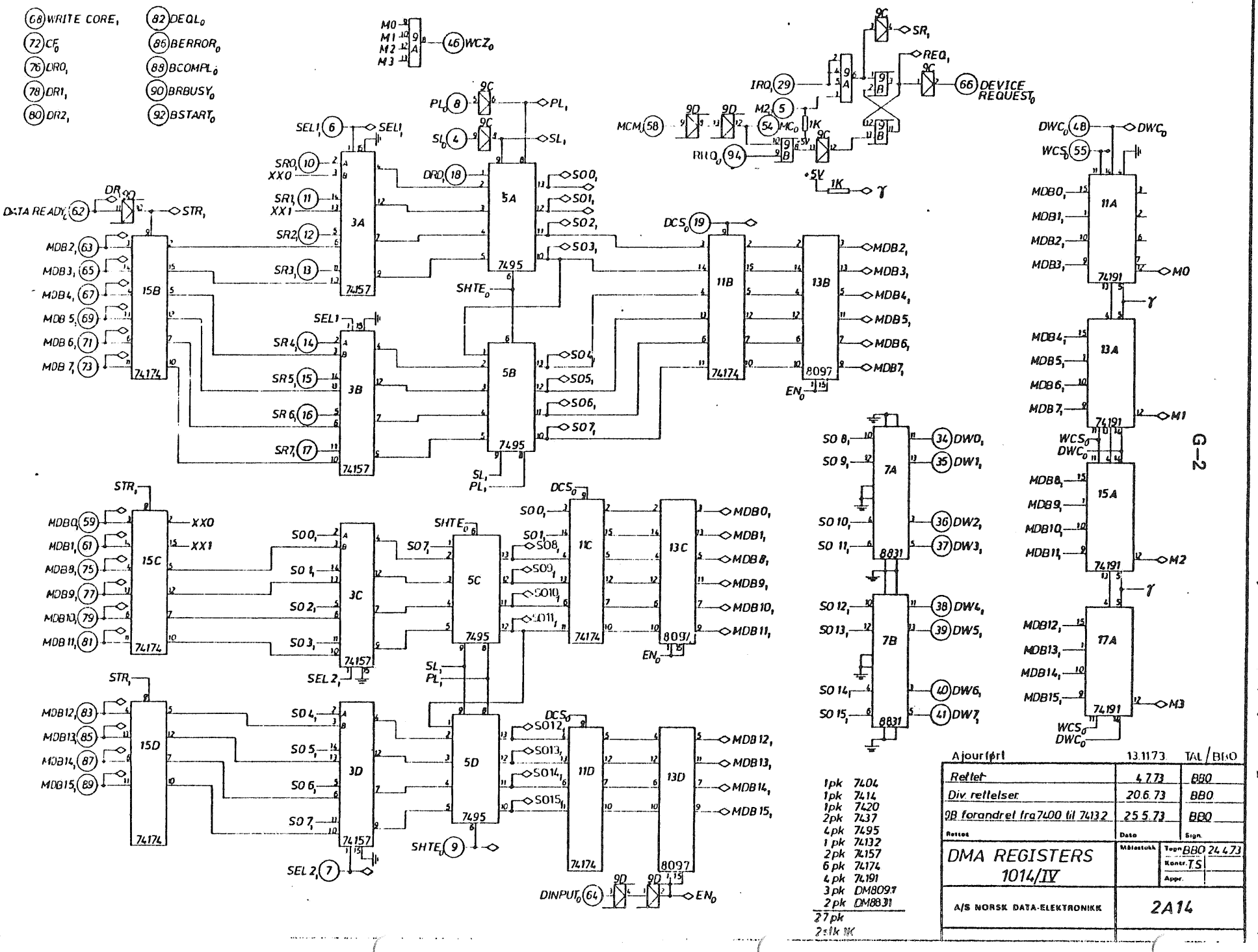
FIGURE 3

APPENDIX G

DRAWINGS

DRAWINGS:

1014	DMA REGISTER
1022	BUS CONTROL
1043	CARD READER BUFFER (DOCUMENTATION)
1093	BRANCH TRANSCEIVER
1095	TERMINAL BUFFER
1096	DMA ADDRESS
1101	BRANCH CONTROL
1119	TRANSCEIVER ADDRESS
1125	TRANSCEIVER DATA
1127	TRANSCEIVER CONTROL
1130	CDC LINEPRINTER INTERFACE



ND-06.012.01

G-2

Forandr. fra 1014 til 1014/IV (ingen rettelser) 7.1.75/TAA/Gml

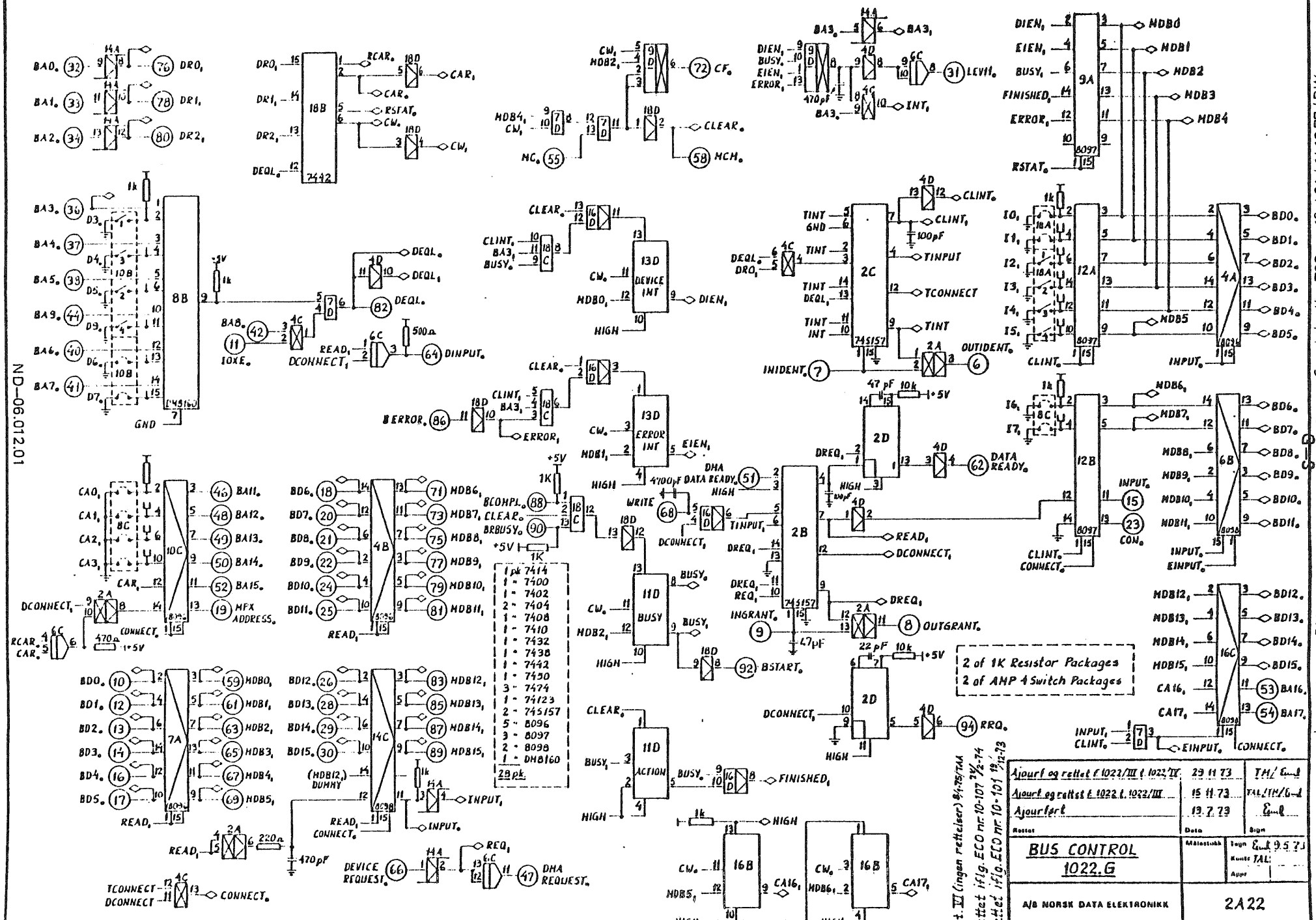
Ajourført	13.11.73	TAL/BBO
Rettet	4.7.73	BBO
Div. rettelser	20.6.73	BBO
9B forandret fra 7400 til 74132	25.5.73	BBO
Rettet	Dato	Sign.

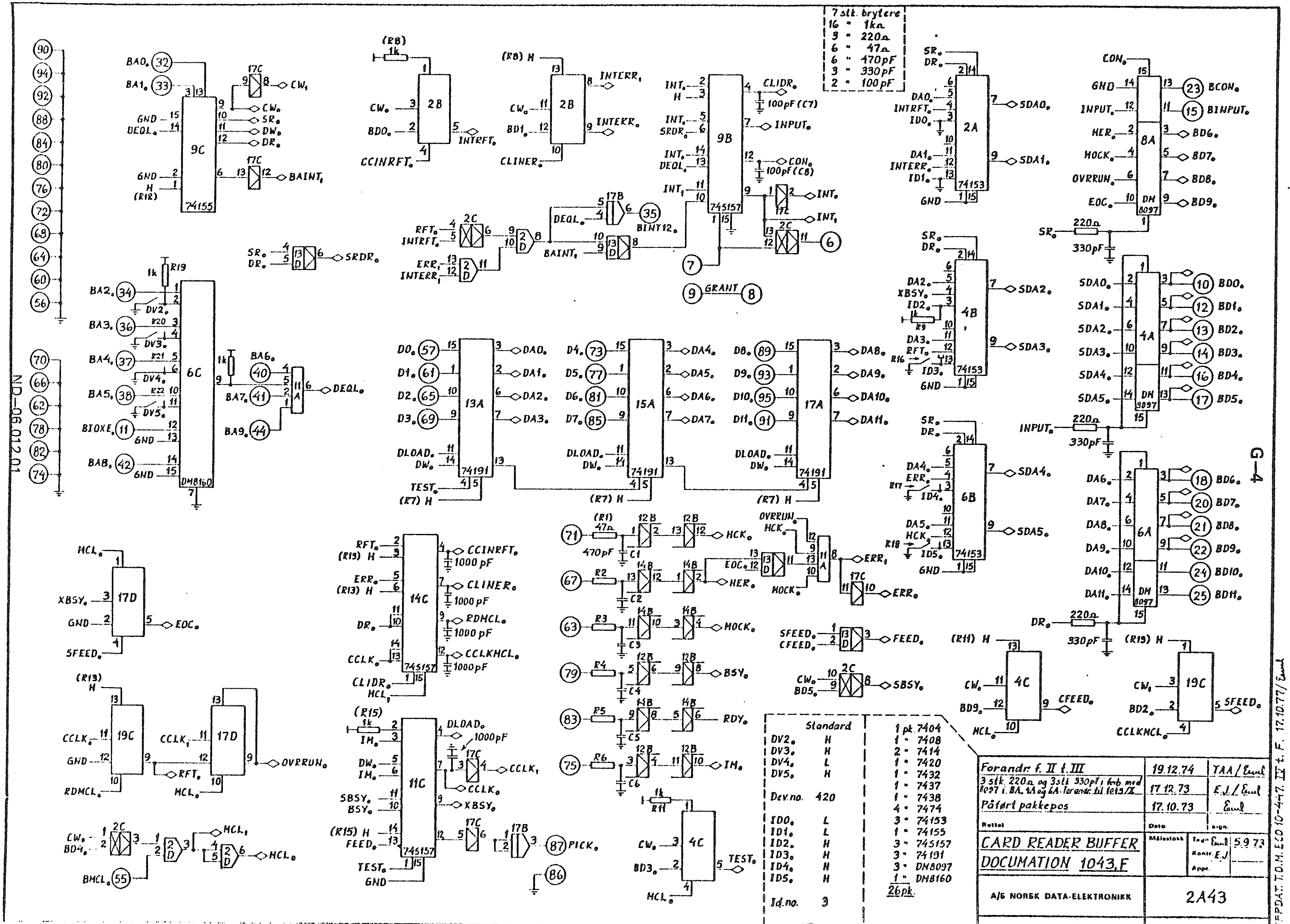
DMA REGISTERS
1014/IV

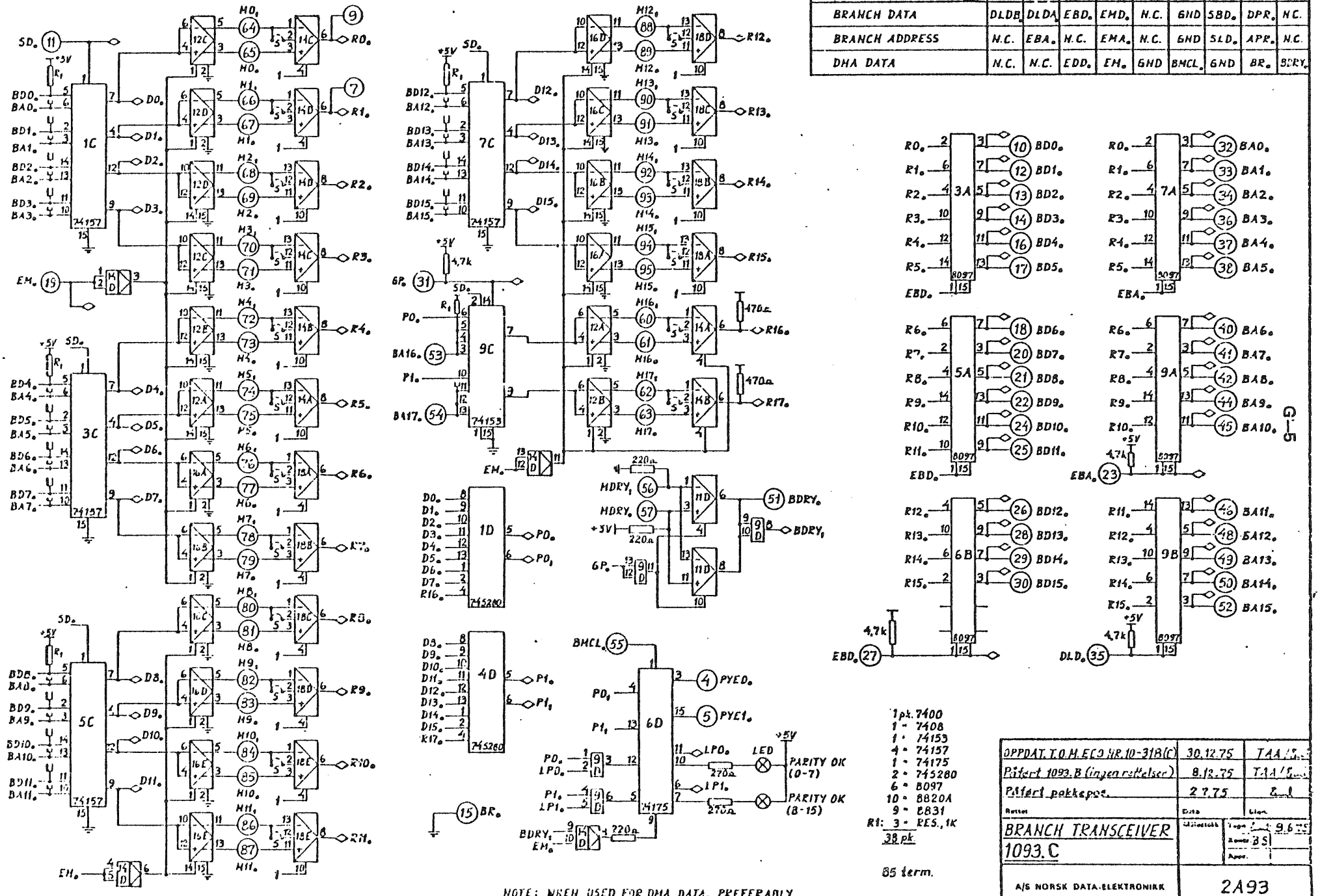
Målestokk | Tegn. BBO 24.4.73 | Kontr. TS | Appr.

A/S NORSK DATA-ELEKTRONIKK

2A14


ND-06.012.01
BUS CONTROL
1022.G
A/S NORSK DATA ELEKTRONIKK
2A22
2 of 1K Resistor Packages
2 of AMP 4 Switch Packages
Ajourf og rettet f 1022/III t 1022/IV 29 11 73 TM/
Ajourf og rettet f 1022 t 1022/III 15 11 73 TAL/TM/
Ajourført 13 7 73
Rettet Dato Sign
Målestokk
Tegn 19 5 73
Kontr TAL
Appr
Oppdat. iflg. ECO nr 10-461 / 14.12.77 / BW
Oppdat. i.o.m. ECO nr. 10-376. III til G. 14/9/77 /
Ajourf. 10.4.75/TAL/
Rettet iflg. ECO nr. 10-101 19/12-73
Rettet iflg. ECO nr. 10-107 3/6-74
IV i. III (ingen rettelser) 8/1-75/TAL
BA0.
BA1.
BA2.
DR0,
DR1,
DR2,
18B
7442
RCAR.
CAR.
RSTAT.
CW.
DEQL.
CW,
MDB4,
MC.
72 CF.
CLEAR.
58 MCH.
DIEN,
BUSY.
EIEN,
ERROR,
470pF
INT,
31 LEVII.
9A
MDB0
MDB1
MDB2
MDB3
MDB4
FINISHED.
RSTAT.
8B
BA3.
BA4.
BA5.
BA6.
BA7.
GND
10XE.
BA8.
DCONNECT,
64 DINPUT.
82 DEQL.
13D
DEVICE INT
MDB0,
HIGH
13D
ERROR INT
MDB1,
86 ERROR.
2C
TINT
GND
DEQL,
INT
TCONNECT
TINPUT
CLINT.
100pF
INIDENT.
7
OUTIDENT.
6
12A
4A
MDB5
INPUT.
BD0.
BD1.
BD2.
BD3.
BD4.
BD5.
2D
DREQ.
DATA READY.
62
47 pF
10k
+5V
12B
MDB6,
MDB7,
MDB8,
MDB9,
MDB10,
MDB11,
6B
BD6.
BD7.
BD8.
BD9.
BD10.
BD11.
8C
10C
CA0,
CA1,
CA2,
CA3,
46 BA11.
48 BA12.
49 BA13.
50 BA14.
52 BA15.
19 MFX ADDRESS.
CONNECT.
470Ω
+5V
4B
BD6.
BD7.
BD8.
BD9.
BD10.
BD11.
71 MDB6,
73 MDB7,
75 MDB8,
77 MDB9,
79 MDB10,
81 MDB11,
READ.
BCOMPL.
CLEAR.
BRBUSY.
1K
1pk 7414
1 - 7400
1 - 7402
2 - 7404
1 - 7408
1 - 7410
1 - 7432
1 - 7438
1 - 7442
1 - 7450
3 - 7474
1 - 74123
2 - 745157
5 - 8096
3 - 8097
2 - 8098
1 - DM8160
28 pk
WRITE
68
4700pF
DATA READY.
51
DCONNECT,
TINPUT,
DREQ,
REQ,
INGRANT.
9
47pF
READ,
DCONNECT,
OUTGRANT.
8
11D
BUSY
BUSY.
BUSY,
92 BSTART.
11D
ACTION
FINISHED,
22pF
94 RRQ.
14C
BD12.
BD13.
BD14.
BD15.
83 MDB12,
85 MDB13,
87 MDB14,
89 MDB15,
(MDB12,) DUMMY
INPUT,
INPUT.
7A
BD0.
BD1.
BD2.
BD3.
BD4.
BD5.
59 MDB0,
61 MDB1,
63 MDB2,
65 MDB3,
67 MDB4,
69 MDB5,
READ.
220Ω
470pF
DEVICE REQUEST.
66
REQ,
47 DMA REQUEST.
TCONNECT
DCONNECT
CONNECT.
16B
CA16,
CA17,
HIGH
16C
BD12.
BD13.
BD14.
BD15.
BA16.
BA17.
53
54
EINPUT.
CONNECT.

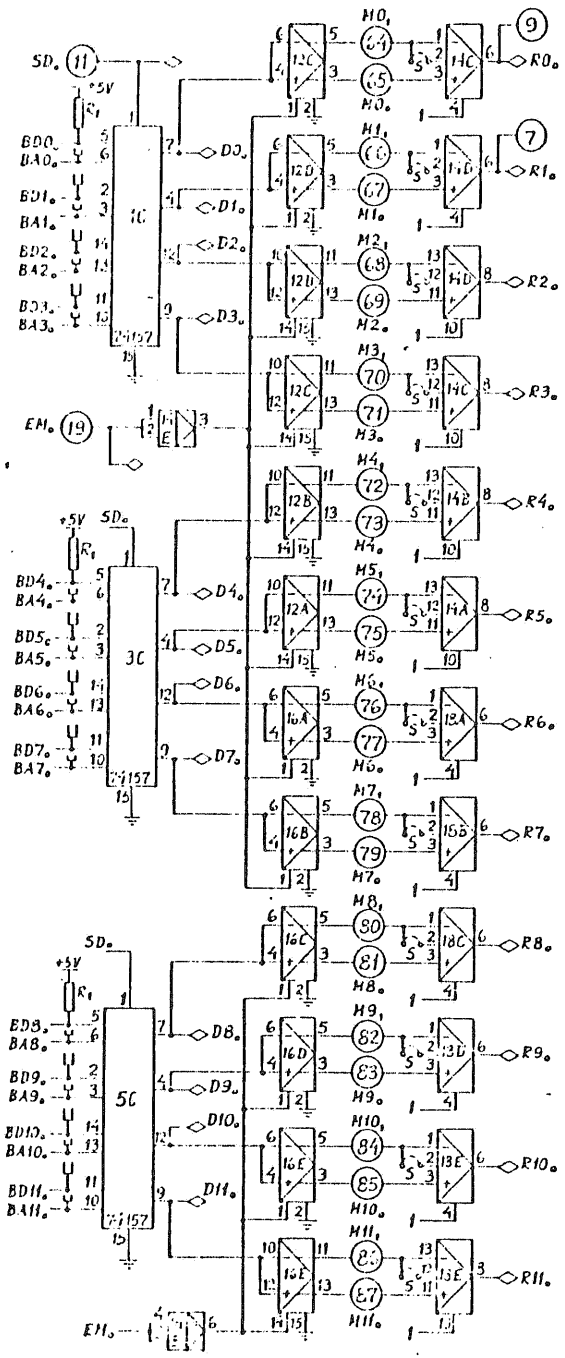

G-4
7 stk. brytere
16 " 1kΩ
3 " 220Ω
6 " 47Ω
6 " 470pF
3 " 330pF
2 " 100pF
Standard
DV2 H
DV3 H
DV4 L
DV5 H
Dev.no. 420
ID0 L
ID1 L
ID2 H
ID3 H
ID4 H
ID5 H
Id.no. 3
1 pk 7404
1 " 7408
2 " 7414
1 " 7420
1 " 7432
1 " 7437
1 " 7438
4 " 7474
3 " 74153
1 " 74155
3 " 745157
3 " 74191
3 " DM8097
1 " DM8160
26pk.
Forandr. f. II t. III
3 stk. 220Ω og 3 stk 330pF i forb. med 8097 i. 8A, 4A og 6A. Forandr. til 1043/II
Påført pakkepos
19.12.74 TAA
17.12.73 E.J.
17.10.73
CARD READER BUFFER
DOCUMATION 1043.F
Tegn. 5.9.73
Kontr. E.J.
A/S NORSK DATA-ELEKTRONIKK
2A43
OPPDAT. T.O.M. ECO 10-447. IV t. F. 17.10.77
ND-06.012.01

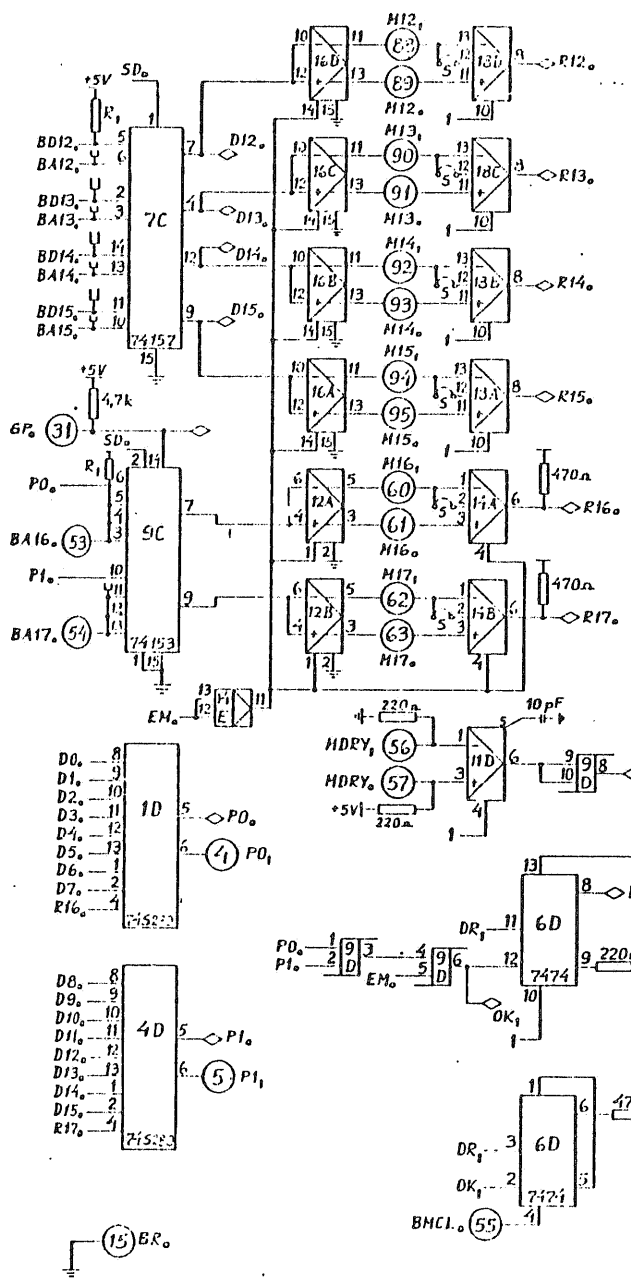

ACTUAL SIGNAL NAMES
USAGE / SIGNAL | DLD. | EBA. | EBD. | EM. | GP. | BMCL. | SD. | BR. | BDRY.
BRANCH DATA | DLDB. | DLDA. | EBD. | EMD. | N.C. | GND | SBD. | DPR. | N.C.
BRANCH ADDRESS | N.C. | EBA. | N.C. | EMA. | N.C. | GND | SLD. | APR. | N.C.
DHA DATA | N.C. | N.C. | EDD. | EM. | GND | BMCL. | GND | BR. | BDRY.
1C
2C
3C
4D
5C
6B
6D
7A
7C
8B
9A
9C
1D
3A
5A
6B
7A
9A
9B
1pk. 7400
1 - 7408
1 - 74153
4 - 74157
1 - 74175
2 - 745280
6 - 8097
10 - 8820A
9 - 8831
R1: 3 - RES., 1K
38 pk
85 term.
NOTE: WHEN USED FOR DMA DATA, PREFERABLY
ND-06.012.01
OPPDAT. T.O.M. ECO NR. 10-318(C) 30.12.75 TAA/S
Påført 1093.B (ingen rettelser) 8.12.75 TAA/S
Påført pakkepos. 2.7.75 Z.I
BRANCH TRANSCEIVER
1093.C
A/S NORSK DATA-ELEKTRONIKK
2A93
G-5

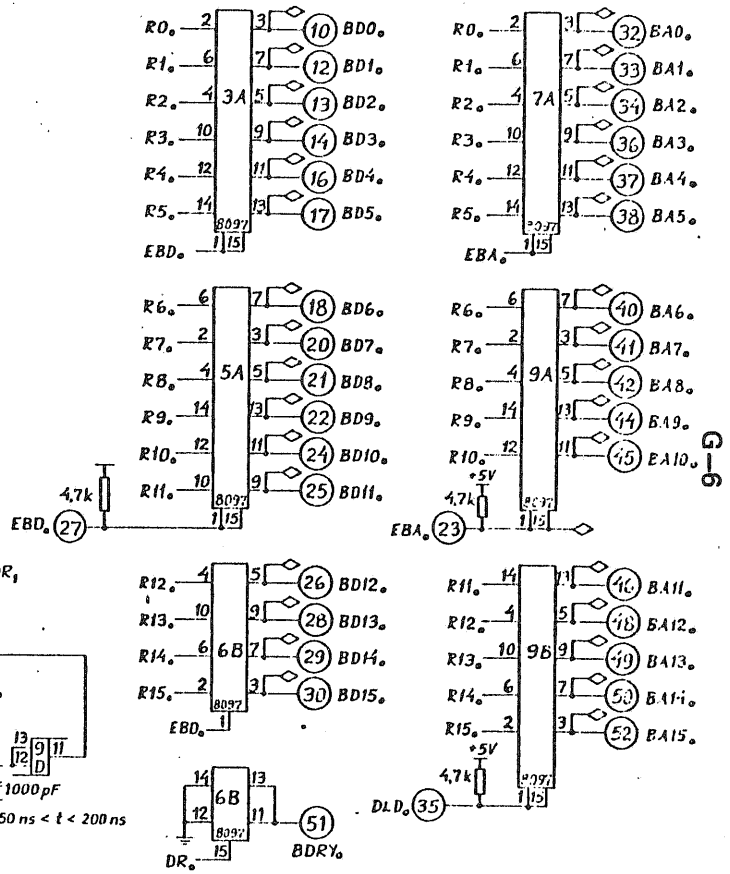
NOTE: WHEN USED FOR DMA DATA, PREFERABLY REMOVE R_1 AND INSERT STRAPS S.

ACTUAL SIGNAL NAMES

USAGE \ SIGNAL	DLD$_0$	EBA$_0$	EBD$_0$	EM$_0$	GP$_0$	BMCL	SD$_0$	BR$_0$	[illegible]
BRANCH DATA	DLDB	DLDA	EBD$_0$	EMD$_0$	N.C.	GND	SBD$_0$	DPR	N.C.
BRANCH ADDRESS	N.C.	EBA$_0$	N.C.	EMA$_0$	N.C.	GND	SLD$_0$	APR	N.C.
DMA DATA	N.C.	N.C.	EDD$_0$	EM$_0$	GND	BMCL	GND	BR$_0$	[illegible]







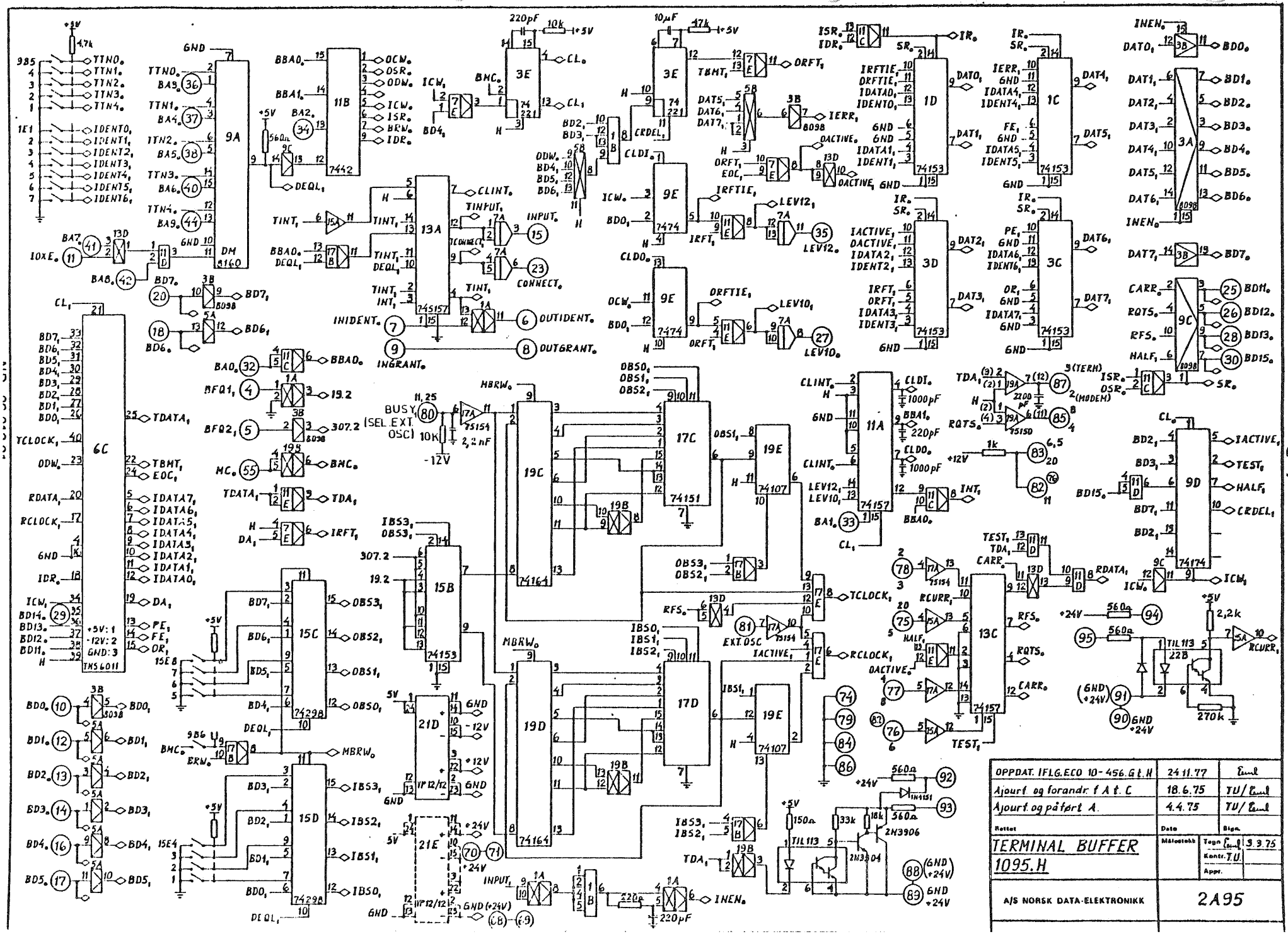
1 pk. 7408
1 " 7474
1 " 74132
1 " 74153
4 " 74157
2 " 745280
6 " 8097
10 " 8820A
9 " 8831
R1: 3 " PLS., 1K
38 pk

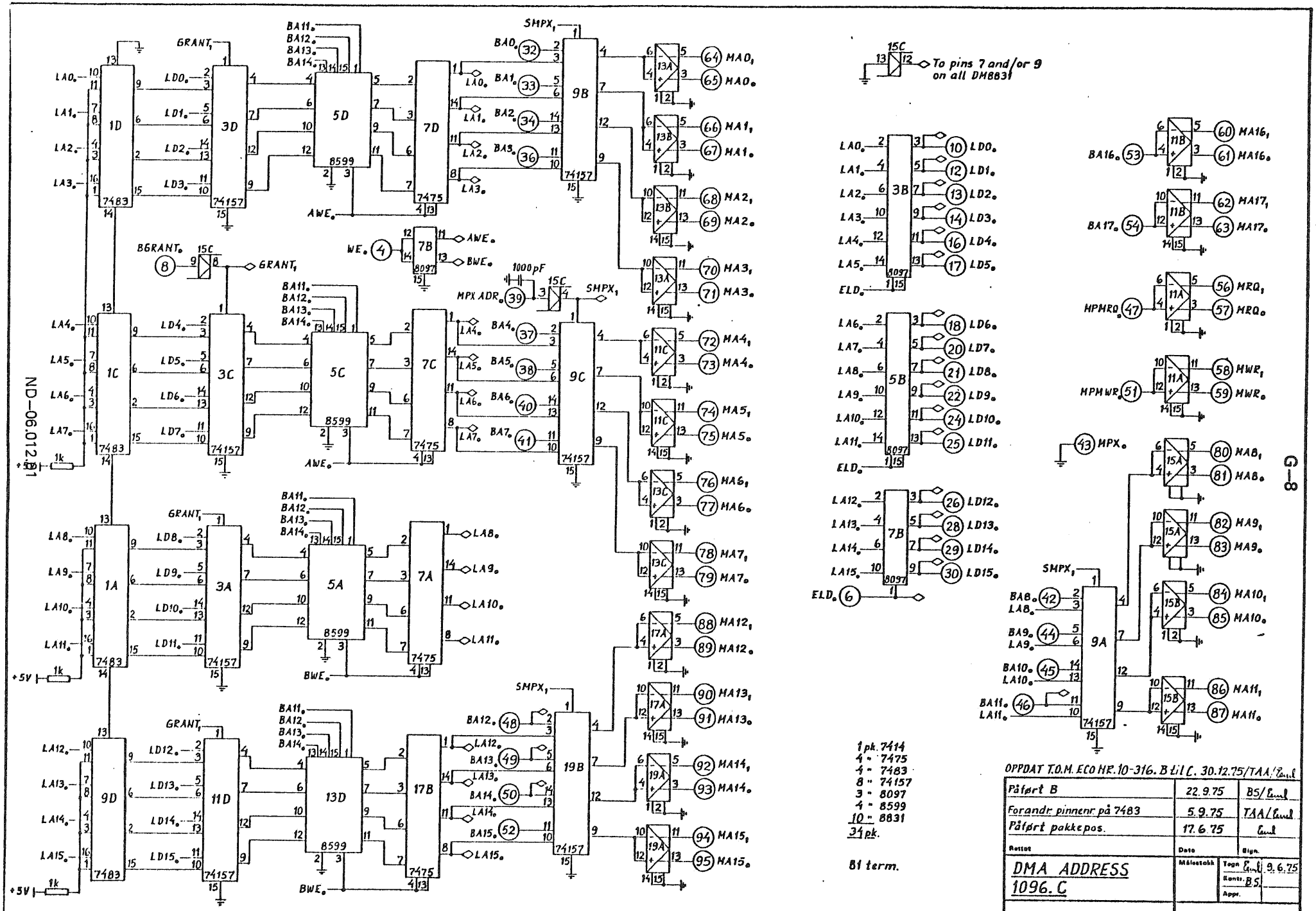
85 term.

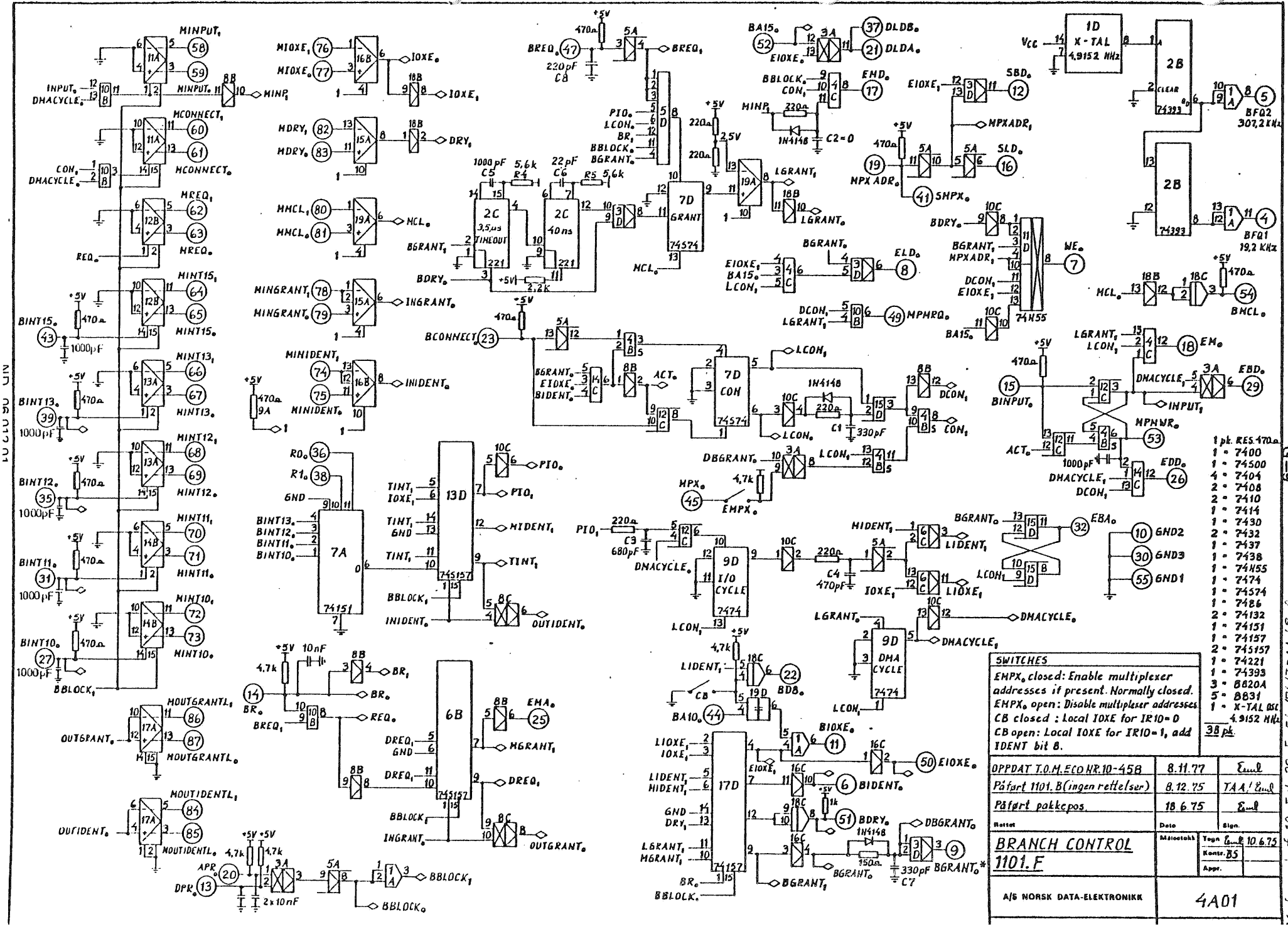
DPPDAT. T.O.M. ECD 10-454. F	17.10.77	Emil
Rettet	Dato	
BRANCH TRANSCEIVER 1093. E, F	Tegningsnr.	
A/S NORSK DATA-ELEKTRONIKK	2A93	

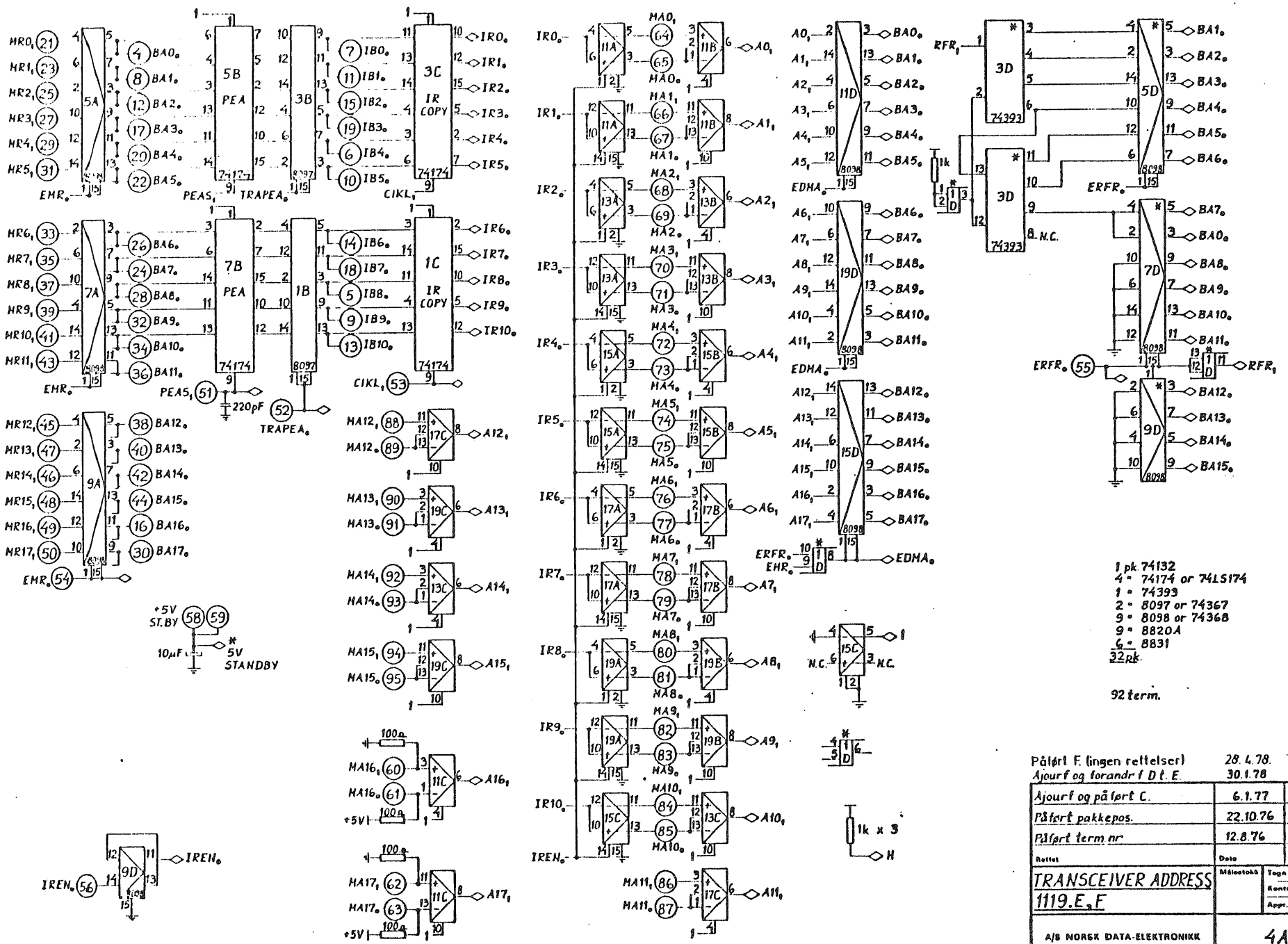
ND-06.012.01

G-6


TERMINAL BUFFER
1095.H
A/S NORSK DATA-ELEKTRONIKK
2A95
OPPDAT. IFLG.ECO 10-456.G.t.H 24.11.77
Ajourf. og forandr. f A.t. C 18.6.75
Ajourf. og påført A. 4.4.75
Rettet Dato Sign.
Målestokk
Tegn
Kontr. T.U.
Appr.
9.9.75
G-7


ND-06.012.01
1D
3D
5D
7D
9B
1C
3C
5C
7C
9C
1A
3A
5A
7A
9D
11D
13D
17B
19B
7B
8599
74157
7483
7475
8097
1k
+5V
GRANT1
BGRANT0
AWE0
BWE0
WE0
SMPX1
MPX ADR0
1000pF
15C
To pins 7 and/or 9 on all DM8831
3B
5B
7B
9A
11B
11A
15A
15B
13A
13B
13C
17A
19A
MPX0
HPMRQ0
HPMWR0
1 pk. 7414
4 = 7475
4 = 7483
8 = 74157
3 = 8097
4 = 8599
10 = 8831
34 pk.
81 term.
OPPDAT T.O.M. ECO NR. 10-316. B til C. 30.12.75/TAA/Emil
Påført B 22.9.75 BS/Emil
Forandr pinnenr på 7483 5.9.75 TAA/Emil
Påført pakkepos. 17.6.75 Emil
Rettet Dato Sign.
DMA ADDRESS
1096. C
Målestokk
Tegn Emil 9.6.75
Kontr. BS
Appr.
A/S NORSK DATA-ELEKTRONIKK
2A96
G-8


SWITCHES
EMPX₀ closed: Enable multiplexer addresses if present. Normally closed.
EMPX₀ open: Disable multiplexer addresses
CB closed: Local IOXE for IR10=0
CB open: Local IOXE for IR10=1, add IDENT bit 8.
1 pk. RES. 470Ω
1 - 7400
1 - 74500
4 - 7404
2 - 7408
2 - 7410
1 - 7414
1 - 7430
2 - 7432
1 - 7437
1 - 7438
1 - 74155
1 - 7474
1 - 74574
1 - 7486
2 - 74132
1 - 74151
1 - 74157
2 - 745157
1 - 74221
1 - 74393
3 - 8820A
5 - 8831
1 - X-TAL OSC 4.9152 MHz
38 pk.
OPPDAT T.O.M. ECO NR. 10-458 8.11.77 Emil
Påført 1101.B (ingen rettelser) 8.12.75 TAA/Emil
Påført pakkepos. 18.6.75 Emil
Rettet Dato Sign.
BRANCH CONTROL
1101.F
Målestokk
Tegn Emil 10.6.75
Kontr. BS
Appr.
A/S NORSK DATA-ELEKTRONIKK
4A01
6-5
6 forandr. f. 10 pF ± 22 pF. 5/1/76/TEAA/Emil



1 pk 74132
4 = 74174 or 74LS174
1 = 74393
2 = 8097 or 74367
9 = 8098 or 74368
9 = 8820A
6 = 8831
32 pk.

92 term.

Påført F. (ingen rettelser)	28.4.78.	TEAA/BW
Ajourf og forandr f D.t.E.	30.1.78	HS/E...8
Ajourf og påført C.	6.1.77	HS/E...8
Påført pakkepos.	22.10.76	HS/E...8
Påført term nr	12.8.76	HS/E...8
Rettet	Dato	Sign.

TRANSCEIVER ADDRESS
1119.E.F

Målestokk | Tegn E... 14.5.76 | Kontr BS | Appr.

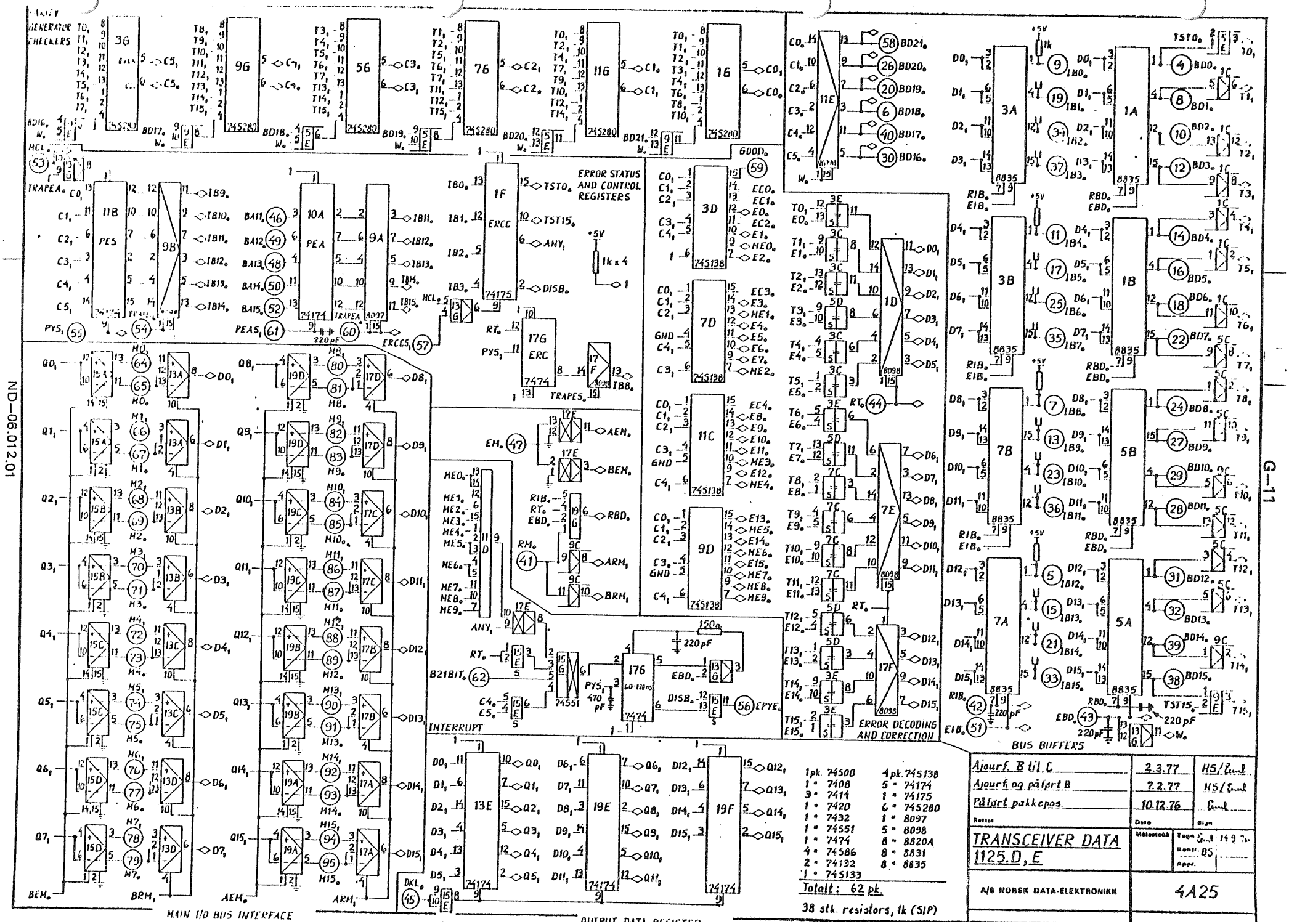
A/S NORSK DATA-ELEKTRONIKK

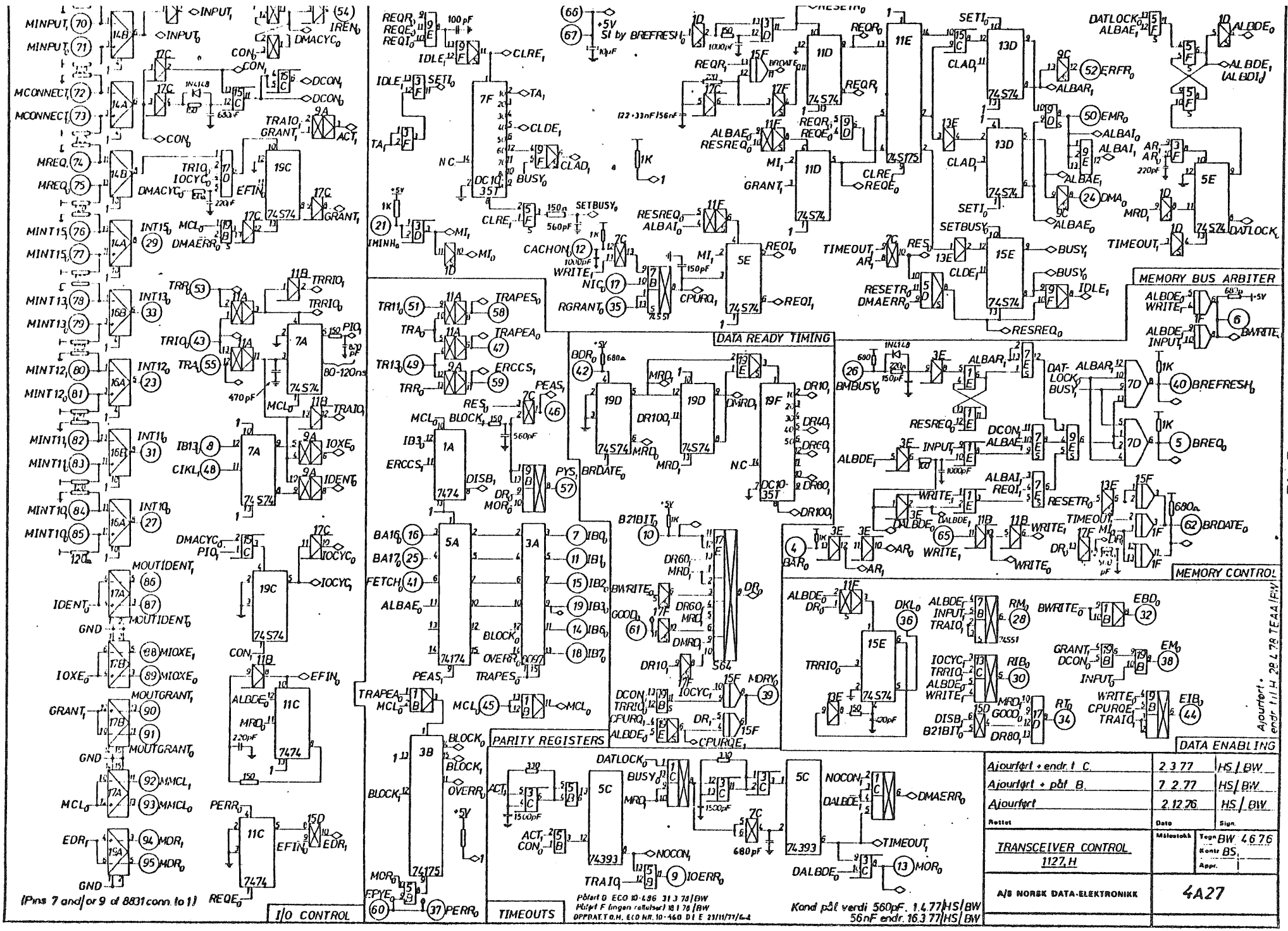
4A19

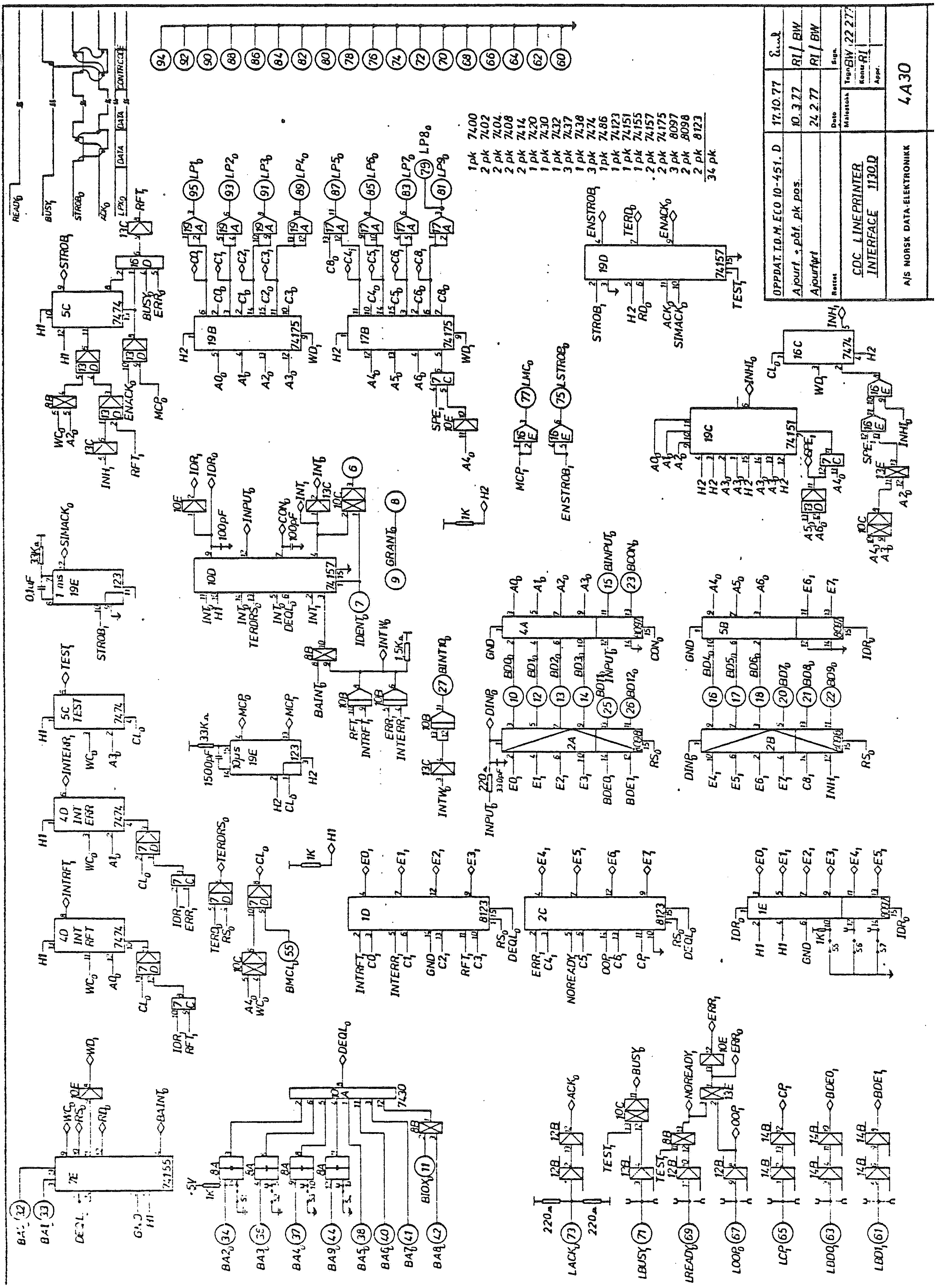
OPPDAT T.D.M.ECO 10-440. 15/9/77/E...8

ND-06.012.01

C-10


PARITY GENERATOR CHECKERS
36
96
56
76
116
16
745280
11E
3D
7D
11C
9D
745138
1F
ERCC
74175
17G
ERC
74174
74474
11B
PES
9B
10A
PEA
9A
8097
TRAPEA
TRAPES
ERROR STATUS AND CONTROL REGISTERS
1k x 4
220 pF
3A
1A
3B
1B
7B
5B
7A
5A
8835
BUS BUFFERS
1D
7E
17F
8098
ERROR DECODING AND CORRECTION
15A
13A
15B
13B
15C
13C
15D
13D
19D
17D
19C
17C
19B
17B
19A
17A
MAIN I/O BUS INTERFACE
176
60-130ns
74551
470 pF
150Ω
INTERRUPT
13E
19E
19F
74174
OUTPUT DATA REGISTER
1pk. 74500
1 • 7408
3 • 7414
1 • 7420
1 • 7432
1 • 74551
1 • 7474
4 • 74586
2 • 74132
1 • 745133
1pk. 745138
5 • 74174
1 • 74175
6 • 745280
1 • 8097
5 • 8098
8 • 8820A
8 • 8831
8 • 8835
Totalt: 62 pk.
38 stk. resistors, 1k (SIP)
Ajourf. B til C
2.3.77
HS/Emil
Ajourf. og påført B
7.2.77
HS/Emil
Påført pakkepos
10.12.76
Emil
Rettet
Dato
Sign
TRANSCEIVER DATA
1125.D, E
Målestokk
Tegn. Emil 14 9 76
Kontr. DS
Appr.
A/S NORSK DATA-ELEKTRONIKK
4A25
ND—06.012.01
G—11


I/O CONTROL
PARITY REGISTERS
DATA READY TIMING
MEMORY BUS ARBITER
MEMORY CONTROL
DATA ENABLING
TIMEOUTS
TRANSCEIVER CONTROL 1127,H
A/S NORSK DATA-ELEKTRONIKK
4A27
Tegn BW 4676
Kontr BS
Ajourført + endr. 1 C 2.3.77 HS/BW
Ajourført + pål. B 7.2.77 HS/BW
Ajourført 2.12.76 HS/BW
(Pins 7 and/or 9 of 8831 conn. to 1)
ND-06.012 01
G-12


CDC LINEPRINTER
INTERFACE 1130 D
A/S NORSK DATA-ELEKTRONIKK
4A30

APPENDIX H

NORD-10 I/O SYSTEM HISTORIC OVERVIEW

BASIC I/O CONFIGURATION

NORD 10.001 → NORD 10.140

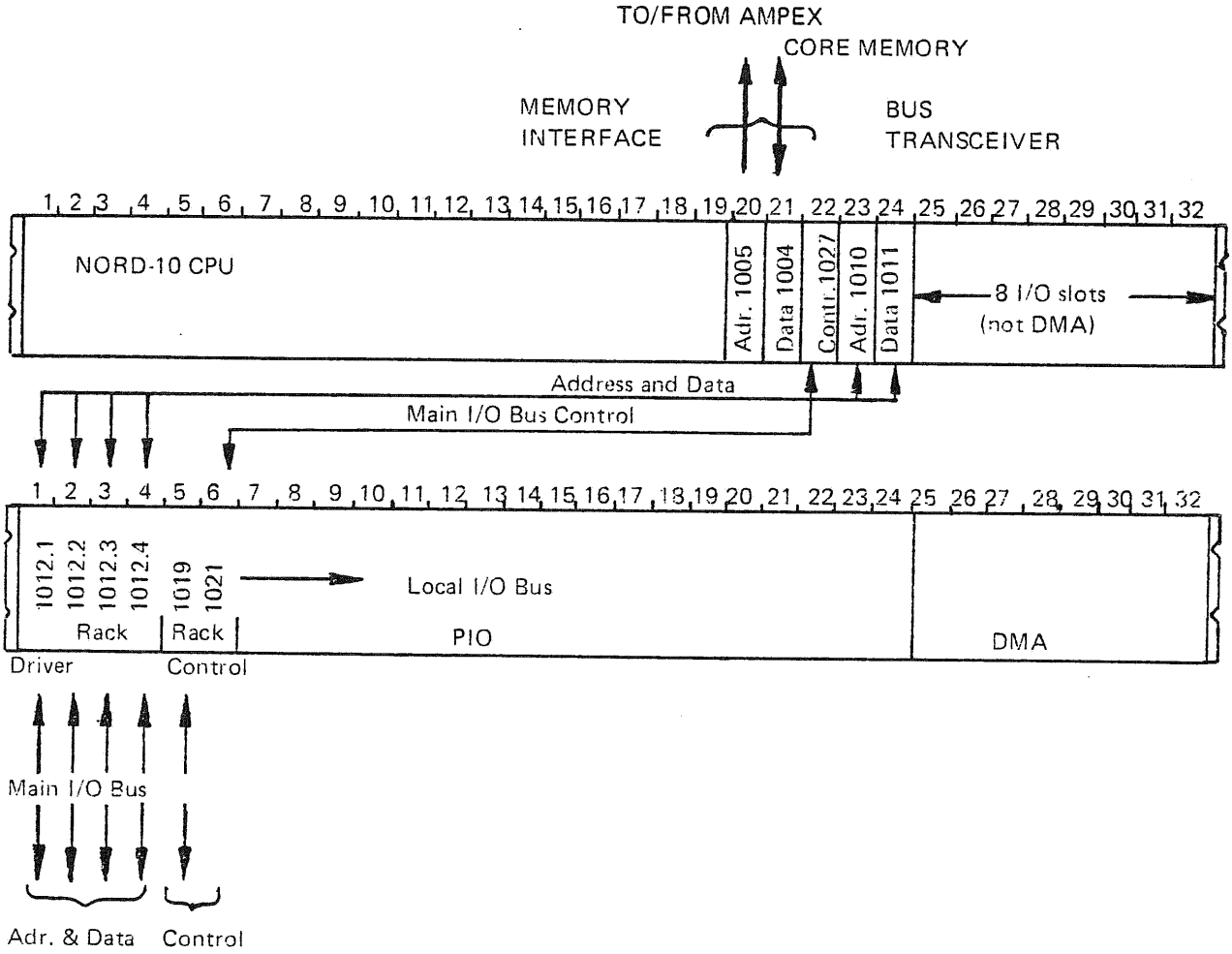


Figure 1.5: TYPICAL I/O CONFIGURATION NORD 10.001 - NORD 10.140

Main differences from N-10S:

- 8 I/O slots for PIO interfaces in the CPU-rack
- Possible to connect-customer equipment via the Main I/O BUS.
- No MPM channel available. All DMA transfer via the CPU.
- One rack-driver module 1012 contains; Drivers/receivers for 4 data and address bits and 4 bits of the Core Address-Register.

MODULE 1012 RACK DRIVER

- Transfer 4 bits of the Main I/O Data-bus MD
- Transfer 4 bits of the Main I/O Address-bus MA
- Convert 4 bits of the MD-bus to local tristate BD-bus
- Convert 4 bits of the MA-bus to local tristate BA-bus
- Contains 4 bits of the Core Address-Register
- Contains 4 bits of UPPER and LOWER address limit-register (Normally disabled)

Bit 0-3	4–7	8–11	12–15
1012.1	1012.2	1012.3	1012.4

MODULE 1019 RACK CONTROL 1

- Priority network for External/Local INTERRUPT and REQUEST
- Circuits for receiving/sending external control signals:

  (CONNECT, INPUT, REQUEST / IDENT, DRY, MCL)

MODULE 1021 RACK CONTROL 2

- Drivers/receivers for control signals to/from CPU
- Drivers/receivers for control signals to/from next I/O-rack
- Protect-registers address decoding
- Terminal oscillator generation (BFQ1 and BFQ2)

NORD 10.141 — NORD 10.299

The multiport-memory system, introducing the MOS-memory was designed in the summer 1975. To live up to the name of a DMA-transfer for mass storage interfaces, the BUS RECEIVER/BRANCHER was designed. Built into the system, is the possibility to perform a true Direct Memory Access. (The BUS BRANCHER.

Main differences from N-10/S:

- 8 I/O slots for PIO interfaces in the CPU-rack
- No Local Memory
- No Cache Memory
- During the DMA transfer via CPU, data is passed via the CPU data bus IB

BASIC I/O CONFIGURATION

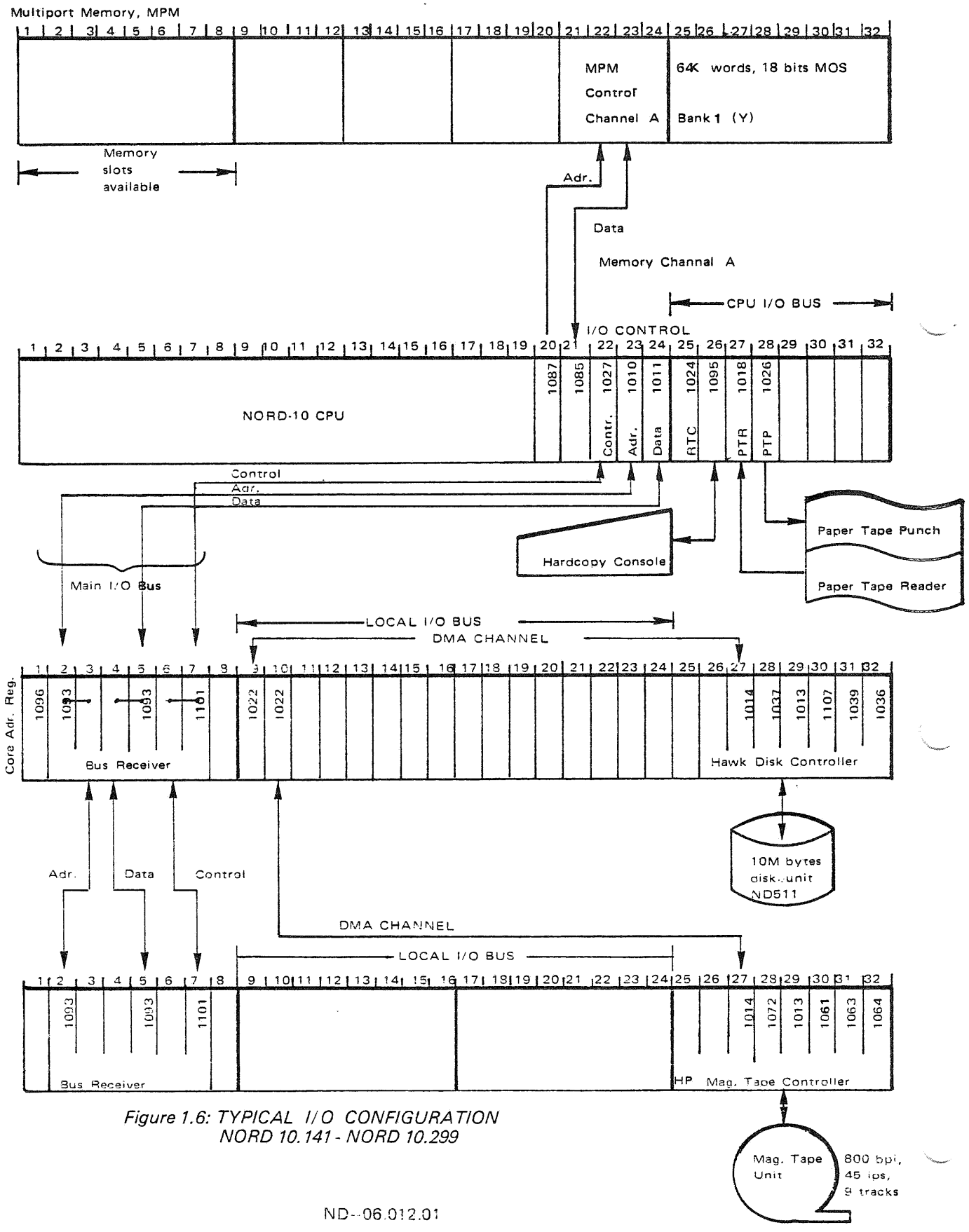


Figure 1.6: TYPICAL I/O CONFIGURATION NORD 10.141 - NORD 10.299

BASIC I/O CONFIGURATION

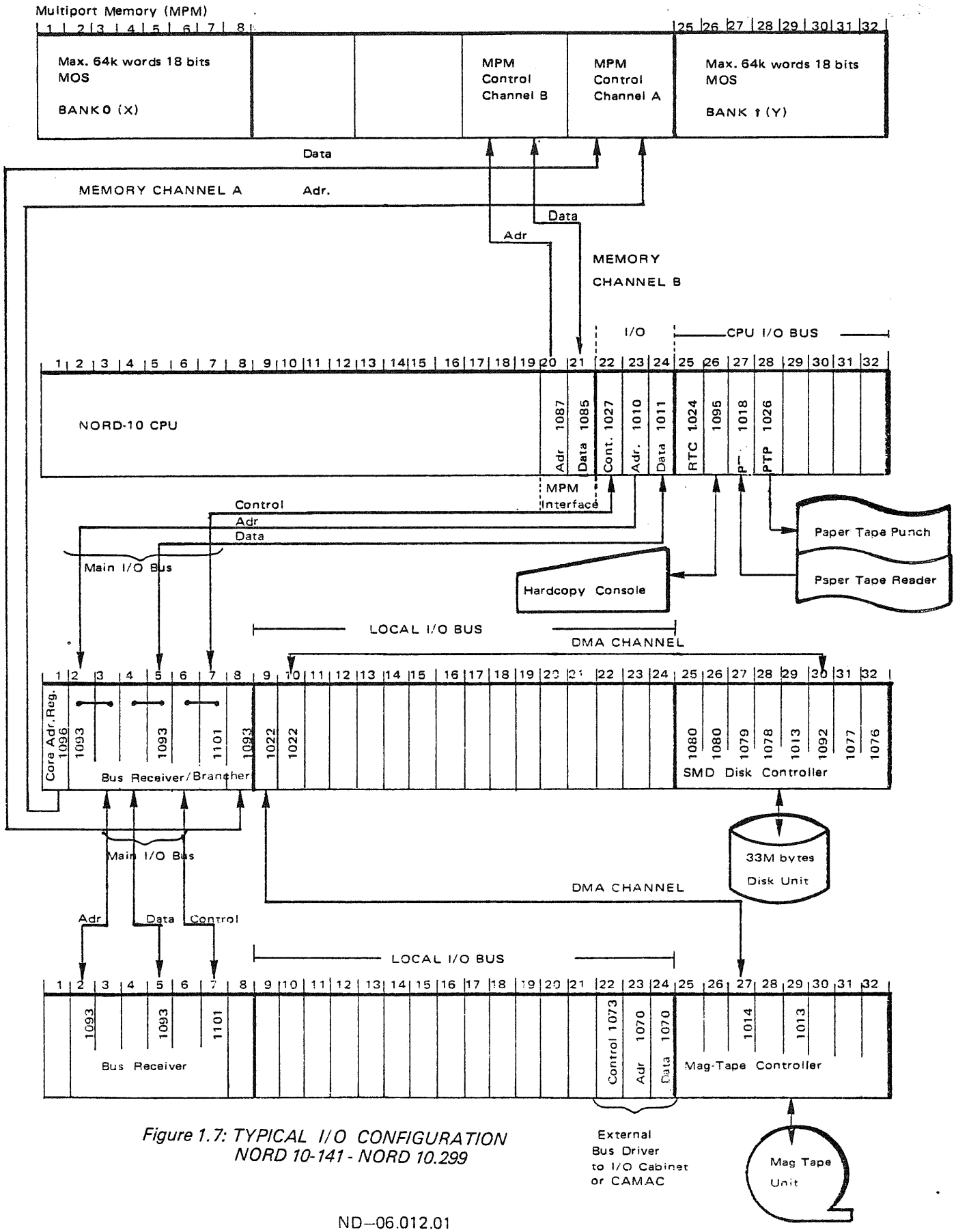


Figure 1.7: TYPICAL I/O CONFIGURATION NORD 10-141 - NORD 10.299

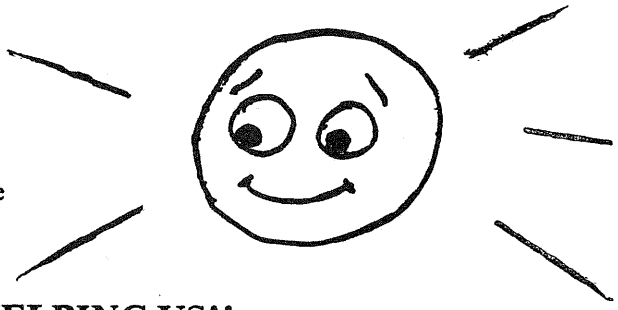
* * * * * * * * * * SEND US YOUR COMMENTS!!! * * * * * * * * * *

Are you frustrated because of unclear information in this manual? Do you have trouble finding things? Why don't you join the Reader's Club and send us a note? You will receive a membership card - and an answer to your comments.

Please let us know if you

* find errors
* cannot understand information
* cannot find information
* find needless information

Do you think we could improve the manual by rearranging the contents? You could also tell us if you like the manual!!



* * * * * * * * * HELP YOURSELF BY HELPING US!! * * * * * * * * *

Manual name: NORD-10/S INPUT/OUTPUT SYSTEM Manual number: ND-06.012.01

What problems do you have? (use extra pages if needed) _____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

Do you have suggestions for improving this manual? _____

_____

_____

_____

_____

_____

_____

_____

_____

Your name: _____ _____ _____ Date: _____

Company: _____ _____ _____ Position: _____

Address: _____

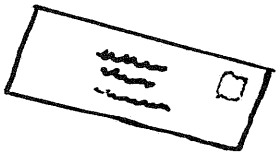
_____

What are you using this manual for? _____

_____

_____

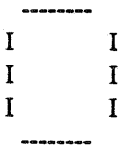
Send to: Norsk Data A.S.
Documentation Department
P.O. Box 4, Lindeberg Gård
Oslo 10, Norway



Norsk Data's answer will be found on reverse side

Answer from Norsk Data _____

Answered by _____ _____ _____ _____ Date _____



Norsk Data A.S.
Documentation Department
P.O. Box 4, Lindeberg Gård
Oslo 10, Norway

– we make bits for the future

NORSK DATA A.S BOX 4 LINDEBERG GARD OSLO 10 NORWAY PHONE: 30 90 30 TELEX: 18661