NORD-10/S

General Description
and
Module Description

NORSK DATA A.S

NORD-10/S

General Description
and
Module Description

REVISION RECORD

Revision	Notes
10/78	ORIGINAL PRINTING

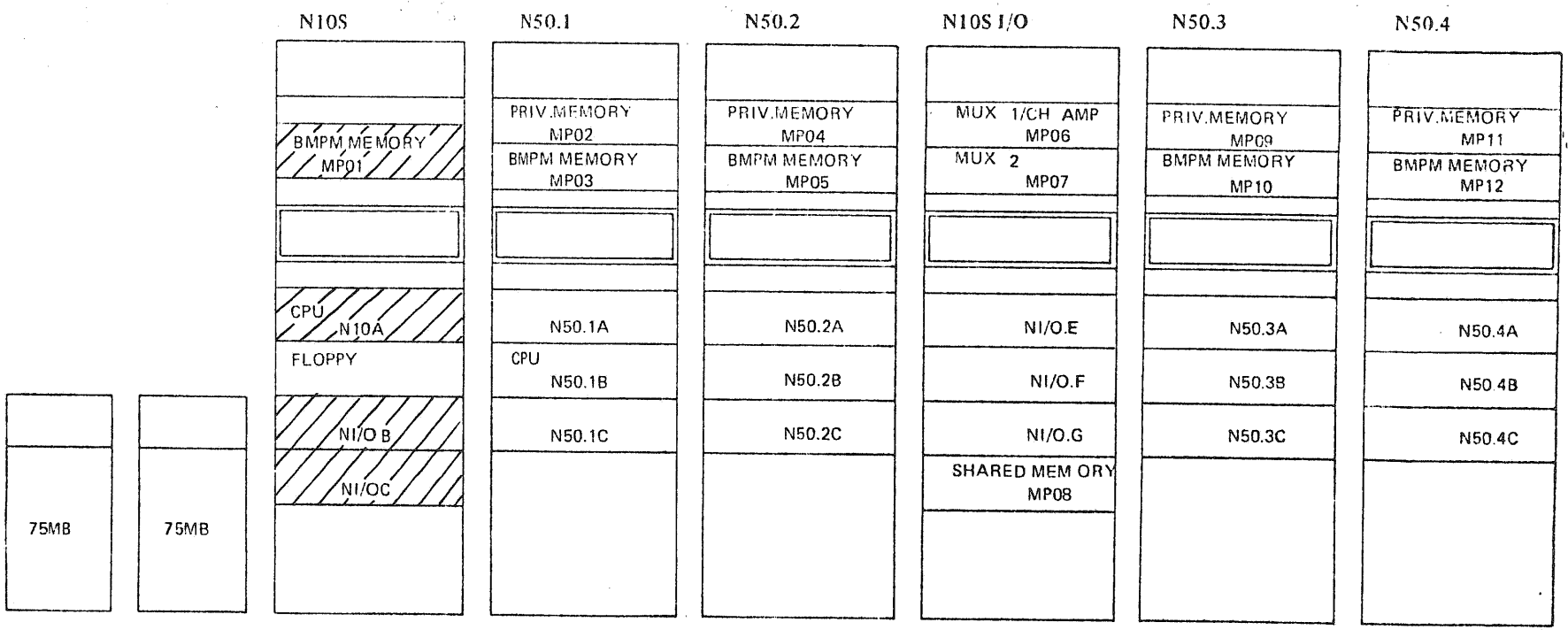
NORD-10/S General Description
Publication No. ND-06.013.01

NORSK DATA A.S
Postboks 4, Lindeberg gård
Oslo 10, Norway

TABLE OF CONTENTS

+ + +

SYSTEM CONFIGURATION F16



NO—06.013.01

1 INTRODUCTION

NORD-10/S is a 16 bit general purpose computer. The maximum address space is 128 Kbytes without the Memory Management System — MMS, and 512 Kbytes with MMS. The Memory Management System offers an efficient paging system including extensive memory protection through a Permit Protect System and a Ring Protect System. A CACHE memory system is also available as an option.

1.1 *INSTRUCTION SET*

The NORD-10/S has instructions which operate on: bit, byte, word, double word, triple word and 8 words equal the whole register block. Integer arithmetical operations include single precision memory to register operations and double precision register to register multiply and divide.

The floating point instructions that add, subtract, multiply and divide use a 32 bit mantissa and a 16 bit exponent (2 bits for sign of exponent and mantissa).

In NORD-10/S — NORD-50 configurations the NORD-10/S floating format equals the NORD-50 single precision format:

- 9 bits exponent
- 23 bits mantissa (fraction with hidden "1" bit)
- 2 bits for sign of exponent and mantissa

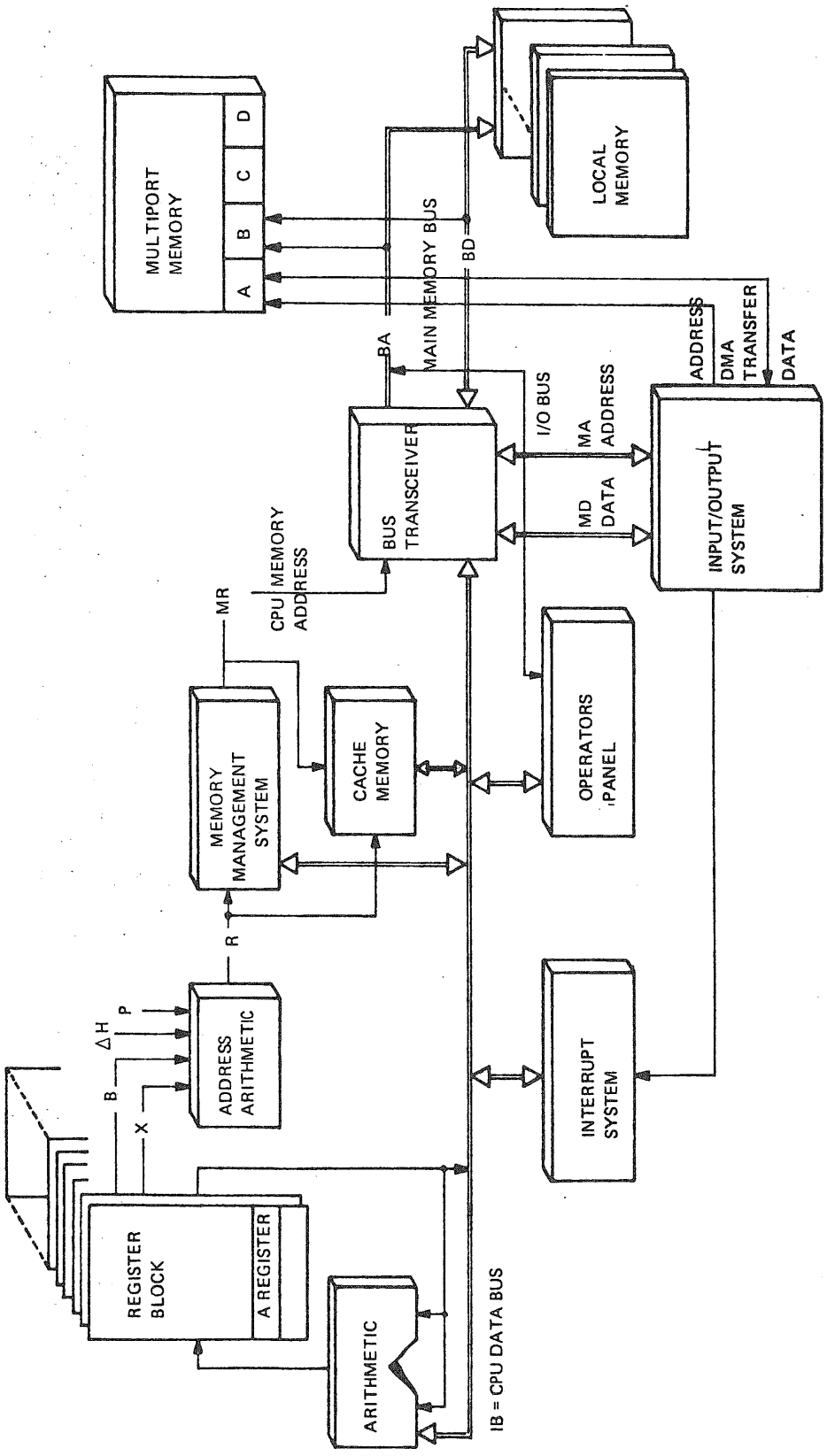
The NORD-10/S is microprogrammed, and all instruction execution is in firmware using a 32 bit Read Only Memory (ROM). To maintain processor speed, the address arithmetic is implemented in hardware which works in parallel with the Read Only Memory access.

The ROM has provisions for user extensions of the NORD-10/S instruction set, by allowing generation of different entry points in the ROM.

ADDRESSING MODES

A variety of addressing modes may be used:

- Program counter relative addressing
- Indirect addressing
- Pre-indexed addressing
- Post-indexed addressing
- Combination of the above mentioned modes


MULTIPORT MEMORY
A
B
C
D
LOCAL MEMORY
BD
MAIN MEMORY BUS
BA
ADDRESS
DMA TRANSFER
DATA
I/O BUS
MA ADDRESS
MD DATA
BUS TRANSCEIVER
INPUT/OUTPUT SYSTEM
CPU MEMORY ADDRESS
MR
MEMORY MANAGEMENT SYSTEM
CACHE MEMORY
OPERATORS PANEL
R
ΔH
P
B
X
ADDRESS ARITHMETIC
INTERRUPT SYSTEM
REGISTER BLOCK
A REGISTER
ARITHMETIC
IB = CPU DATA BUS

1.2 *NORD-10/S MODULE INTERCONNECTIONS*

REGISTER BLOCK	:	Contains 16 Levels of the 8 Program Able Registers
ARITHMETIC	:	Main Arithmetic for Instruction Execution
ADDRESS ARITHMETIC	:	Address Calculation While Executing a Memory Reference Instruction
MEMORY MANAGEMENT SYSTEM	:	Converting the Logical CPU Address (16 Bits) to a Physical 18 Bits Memory Address
INTERRUPT SYSTEM	:	Program Level Activation
OPERATORS PANEL	:	Examine/Deposit the Registers and Memory and Bus Examination
BUS TRANSCEIVER	:	Establish the Communication Between the CPU Address and Data Bus and the Memory Address and Data Bus During: 1. Instruction Fetch 2. Indirect Address Read 3. Memory Operand Read/Write Connect the CPU Data Bus to the I/O Data Bus During an Input/Output Operation
INPUT/OUTPUT SYSTEM	:	Establish Communication With External Devices
MEMORY SYSTEM	:	
CACHE MEMORY	:	Hidden Memory (1K Word) Between the Register Block and the Main-Memory
LOCAL MEMORY	:	Memory Modules Located in One of the Rightmost Positions in the CPU-Rack
MULTIPORT MEMORY	:	Memory Being Accessed From Multiple Sources

1.3 *REGISTER BLOCK*

The CPU has 16 program levels, each level has the following 8 registers:

STS Status (STS). This register holds different Status indicators.

D This register is an extension of the A-register in double precision or floating point operations. It may also be connected to the A-register during double length shifts.

P Program Counter, address of current instruction. This register is controlled automatically in the normal sequencing or branching mode. But it is also fully program controlled and its contents may be transferred to or from other registers.

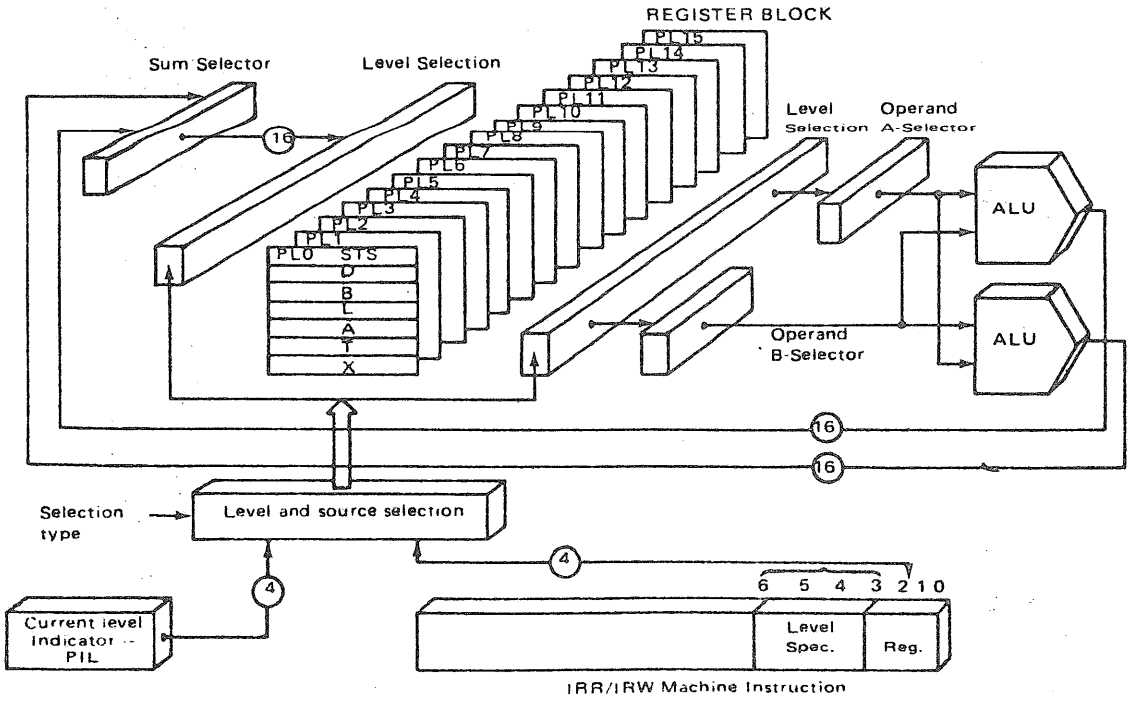
B Base register or second index register. In connection with indirect addressing, it causes preindexing.

L Link register. The return address after a subroutine jump is contained in this register.

A This is the main register for arithmetical and logical operations together with operands in memory. The register is also used for CPU controlled I/O communication.

T Temporary register. In floating point instructions it is used to hold the exponent part. With 32 bits floating format, the exponent is held in the A-register and the mantissa in the A and D-registers.

X Index register. In connection with indirect addressing, it causes post indexing.



1.4 *THE MAIN ARITHMETIC*

The Main Arithmetic consists of two identical 16 bit modules.

During all integer and logical operations only one arithmetic unit is active. For floating point operations, however, the two modules are connected to form a full 32 bit wide arithmetic.

All setting of status flip flops as static and dynamic overflow, carry, etc., is done by the most significant arithmetic module.

The two selectors, A and B are selecting the two operands as inputs to the arithmetic. Both operands are selected at the same time.

The A-operand may be any of the central registers on the current level, status, zero, latched operand from either:

1. Memory
2. Input/Output system
3. Register outside the register block (Internal registers)

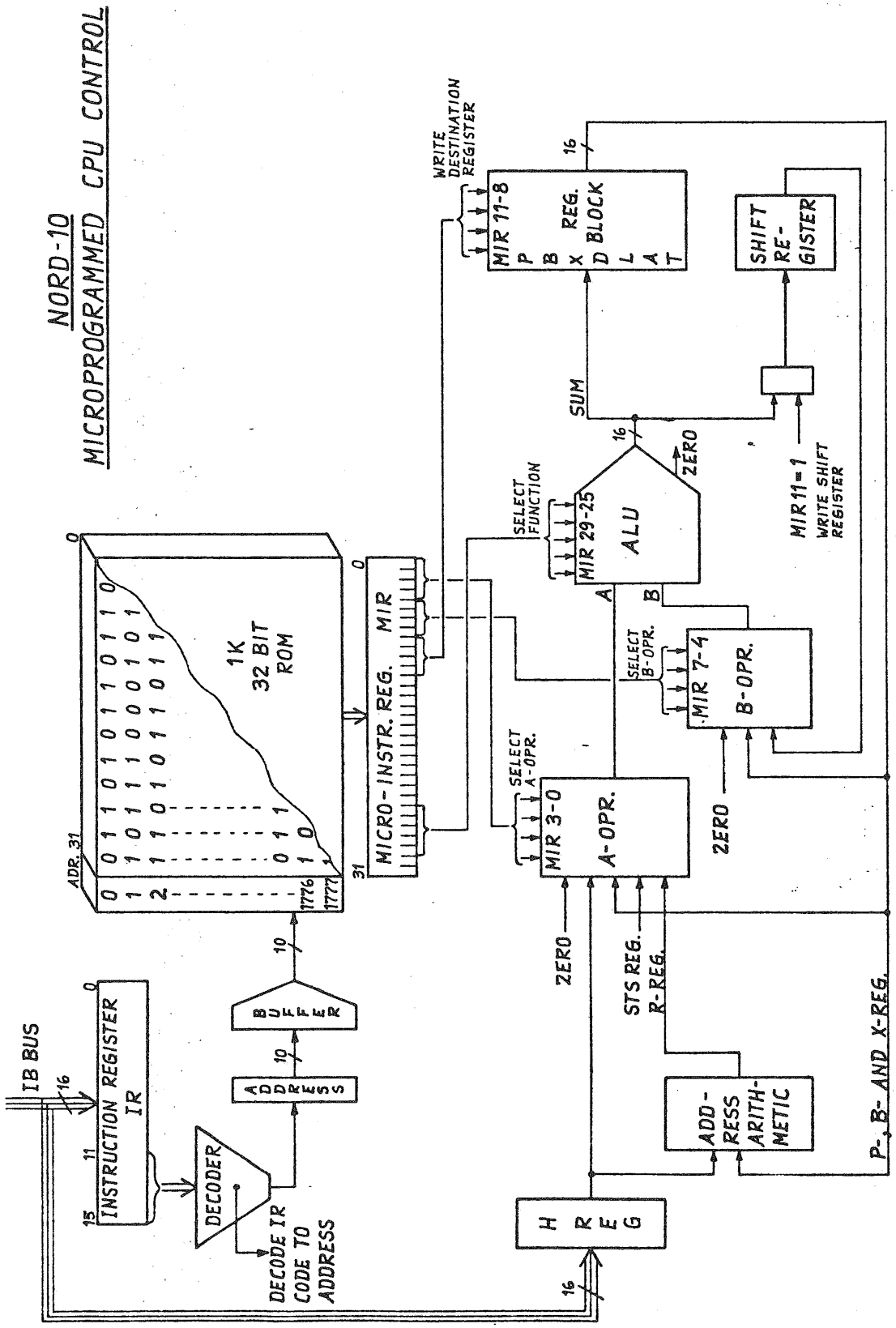
The B-operand may be any of the 8 registers (except STS), zero, bit mask or the temporary result-register AC.

READ ONLY MEMORY (ROM)

The 32 bits wide read only memory can be divided into two main parts:

1. The first part containing control information for instruction execution. Each instruction may occupy from 1 (Argument instruction) to 27 (Integer divide) read only memory locations.

2. The second part contains microcode for servicing the operators communication either via the panel or the terminal 1 in stop mode.


NORD-10
MICROPROGRAMMED CPU CONTROL
IB BUS
INSTRUCTION REGISTER IR
DECODER
DECODE IR CODE TO ADDRESS
ADDRESS
BUFFER
1K 32 BIT ROM
ADR. 31
MICRO-INSTR. REG. MIR
WRITE DESTINATION REGISTER
MIR 11-8
PB REG. X BLOCK LATCH
SHIFT REGISTER
SUM
SELECT FUNCTION
MIR 29-25
ALU
ZERO
MIR 11=1
WRITE SHIFT REGISTER
SELECT B-OPR.
MIR 7-4
B-OPR.
SELECT A-OPR.
MIR 3-0
A-OPR.
2ERO
ZERO
STS REG.
R-REG.
ADDRESS ARITHMETIC
HREG
P-, B- AND X-REG.

1.5 *THE INTERRUPT SYSTEM*

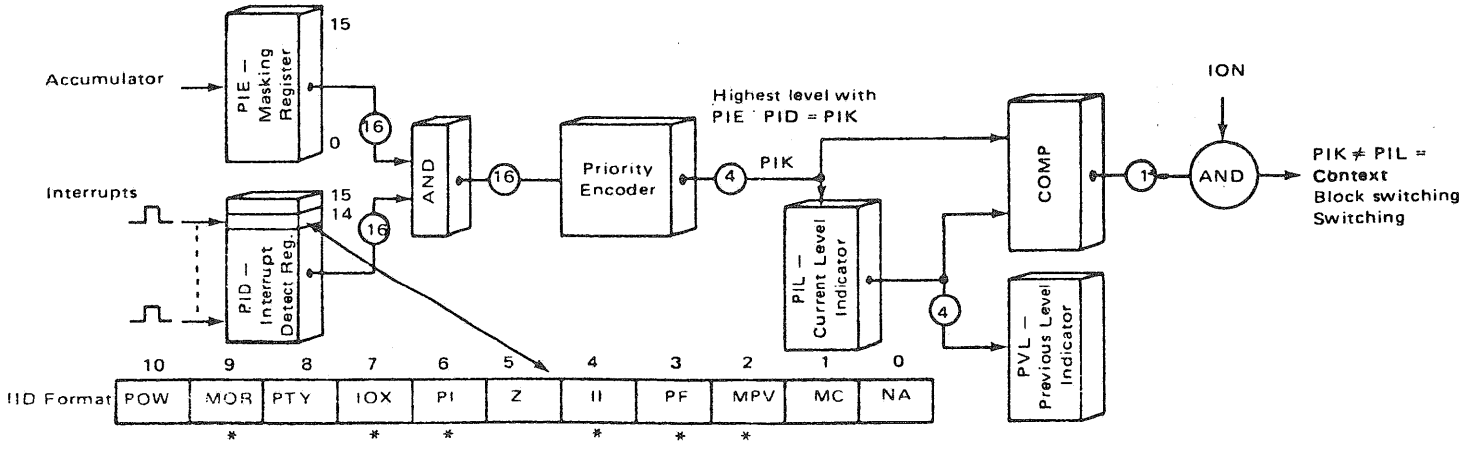
The NORD-10/S has a 16 level priority interrupt system. To each level is assigned a complete set of all the central registers: STS, D, P, B , L, A, T, X. With this architecture, a context block switching is reduced to select the working set of central register. The time required for this operation is 1 μs.

All program levels may be activated by software. In addition, each of the levels 10, 11, 12 and 13 may be activated by 512 vectored I/O interrupts. An IDENT instruction is used to identify the interrupting device. Program level 14 is used by the Internal Interrupt System, which monitors error conditions or traps in the CPU. Program level 15 may only have one I/O interrupt source.

(Program level 15 is not used by standard NORD equipment or software, but is available for users who need an immediate access to the CPU).

The Internal Interrupt System will report 10 different internal conditions:

- MC Monitor Call
- MPV Memory Protect Violation
- PF Page Fault
- II Illegal Instruction (Read Only Memory Timeout)
- Z Error Indicator
- PI Privileged Instruction
- IOX I/O Timeout (No Connect Timeout)
- PTY Parity Error
- MOR Memory Out of Range (Memory Timeout)
- POW Power Fail



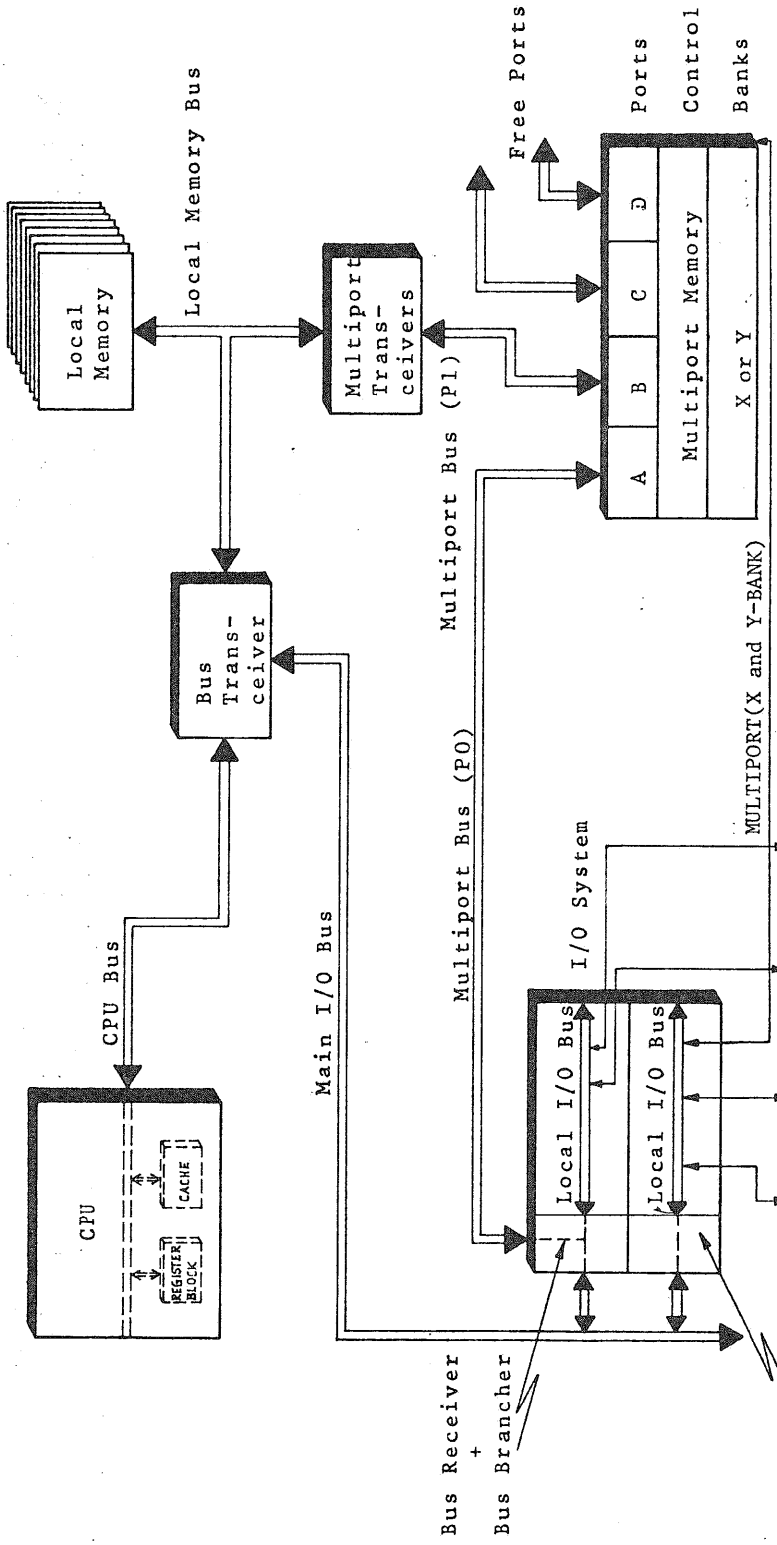
1.6 *THE MEMORY SYSTEM*

The memory system includes:

- 2 Kbytes CACHE memory
- Up to 512 Kbyte local memory, or
- Up to 512 Kbyte Multiport Memory System

OR IN FRENCH:

- 2 Koctets de memoire CACHE
- jusqu a 512 Koctets de memoire locale ou
- jusqu a 512 Koctets en systeme de memoire multiport



Storage Interconnection

1.6.1 *CACHE Memory*

The high speed static CACHE memory is an option that will reduce the average memory access time. The contents of the CACHE hold the most actual data and instructions to be processed.

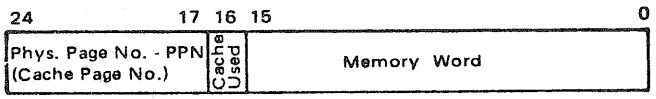
During CPU WRITE, the CACHE is updated in parallel with the MAIN MEMORY access.

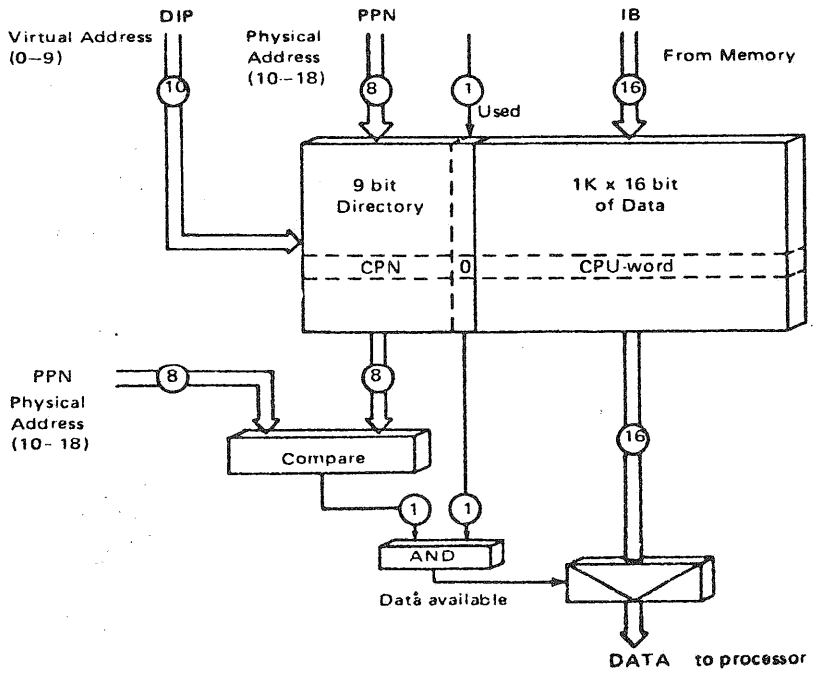
CACHE Memory Architecture

The CACHE Memory is organized as a 1K by 25 bit look-up table. A word in CACHE is identified with the main memory physical address — the physical page number.

The CACHE Memory is homogeneous, i.e., the CACHE Memory does not discrimate between data words, instructions or indirect addresses stored in the main memory.

Each word in the CACHE Memory has the following format:





CACHE Inhibit Area

The CACHE Memory System contains two 8 bit registers which define a contiguous area in memory which will NOT be copied into CACHE when accessed. The inhibited area includes all pages with:

$$\text{Lower limit} \leqslant \text{PPN} \leqslant \text{Upper limit}$$

The inhibit features are intended for use on memory areas that are operated upon by high-frequency DMA transfers and/or parallel processors, to ensure that the CPU does not operate on stale data which otherwise could reside in CACHE.

1.6.2 *Local Memory*

The Local Memory is physically located next to the CPU in the A-rack where 8 slots are reserved. Maximum memory size is 512 Kbytes (8 modules of 64 Kbytes X 21 bits each).

- A single bit error occurring on a 21 bit module will be corrected and the error may be reported to the Internal Interrupt System
- Multiple bit errors occurring on a 21 bit module will be reported to the Internal Interrupt System which interrupts the CPU

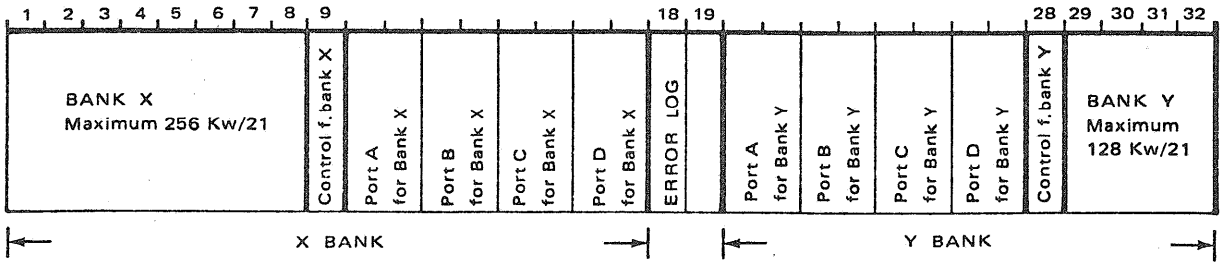
1.6.3 *The Multiport Memory System*

For maximum flexibility a Multiport System may be used. The Multiport Memory System = 1 card crate consisting of two banks, the X and Y bank.

A bank consists of:

- Storage section (Maximum 512 Kbytes for the X and 256 Kbytes for the Y bank)
- Control section, including timing, priority-network and refreshing
- Up to 4 ports through which 4 sources may access the bank

Each port contains error checking and correcting (as for local memory). The error is reported to an ERROR LOG module readable by the NORD-10/S via a special service channel connected to the NORD-10/S Input/Output system.



1.7 *MEMORY MANAGEMENT SYSTEM*

The Memory Management System includes two major subsystems:

— The Paging System
— The Memory Protection System

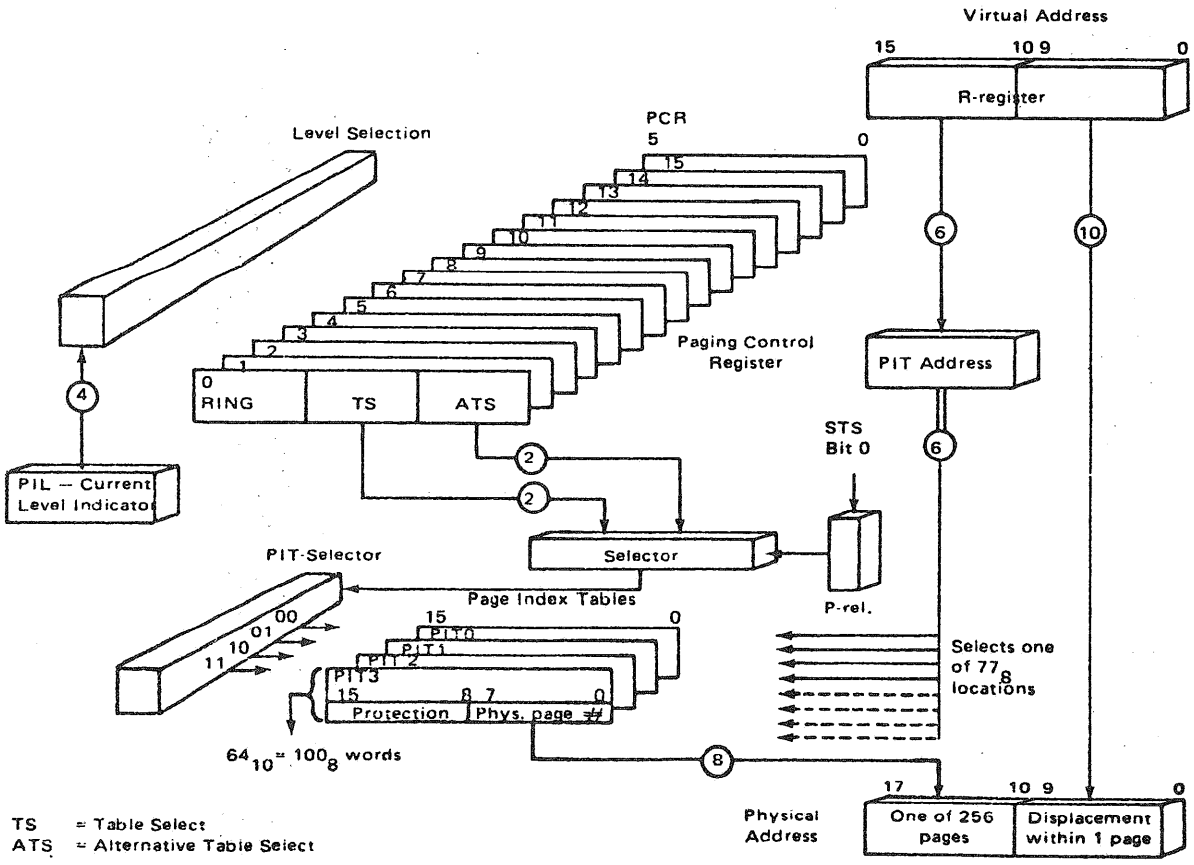
The Paging System maps a 16 bit virtual address into an 18 bit physical address, extending the physical address space from 128 to 512 Kbytes. Four page index tables of 64 words each, located in high-speed registers, reduce paging overhead to practically zero. Data and instruction pages may be allocated anywhere in memory without restriction. The page size is 1024 words.

The Memory Protection System may be divided into two subsystems:

— The Page Protection System
— The Ring Protection System

The Page Protection System protects each page from read, write or instruction fetch accesses or any combination of these.

The Ring Protection System places each page on one of four priority rings. A page of memory that is placed on one specific ring may not be accessed by a program that resides in a page on a ring of lower priority. This system is used to protect system programs from user programs, the Operating System from its subsystems, and the system kernel from the Operating System.



1.8 *THE INPUT/OUTPUT SYSTEM*

GENERAL

For data entering or leaving the general-purpose 16 bits computer NORD-10/S there are two possibilities:

1. Via a Programmed Input/Output-interface
2. Via a Direct Memory-Access interface

Both interface types serve the following functions:

- Synchronize the speed of the CPU and the device
- Convert the data to a suitable format before entering or after leaving the physical device

PROGRAMMED INPUT/OUTPUT – (PIO)

The PIO interface is, with a few exceptions, made of one card module. One card for each device, occupies one slot in the I/O rack.

All data and control information is exchanged between registers in the interface and the accumulator of the A-register in the CPU register block. Programmed I/O interfaces are used for all slow serial or byte oriented peripheral devices. Typical: Tape-reader, Card-reader, Line printer, Display, Modem. The data transfer between the A-register and the interface is programmed. A separate Input-Output Execute instruction (IOX) is required to exchange data between the A-register and interface registers. The register-address is given by the 11 lower bits of the IOX-instruction.

DIRECT MEMORY ACCESS – (DMA)

The Direct Memory Access (DMA) channel is used to obtain high transfer rates to and from main memory. CPU and DMA transfers may, therefore, be performed simultaneously.

The Direct Memory-Access interface normally consists of 4 to 12 cards located in the I/O rack. The DMA interface transfers blocks of data:

- Directly to/from the multiport memory via one separate port
- To/from the local memory in the CPU-rack
- To/from the multiport memory via the CPU port

The two last transfers are based on CPU cycle stealing, while the first transfer takes place simultaneously with the CPU if the CPU and the DMA are accessing different banks. Typical DMA devices are DISKS, DRUMS, PLOTTERS and MAG-TAPES.

More than one DMA device may be active on the DMA channel at the same time, sharing the channel's total band width.

BOOTSTRAP LOADING

Bootstrap Loading is under microprogram control and makes available the following facilities:

— octal or binary load, from character oriented devices, i.e., from Floppy Disk, Paper Tape or communication line

— system loading from block oriented devices, i.e., disk

2 CPU AND LOCAL MEMORY DESCRIPTION

GENERAL:

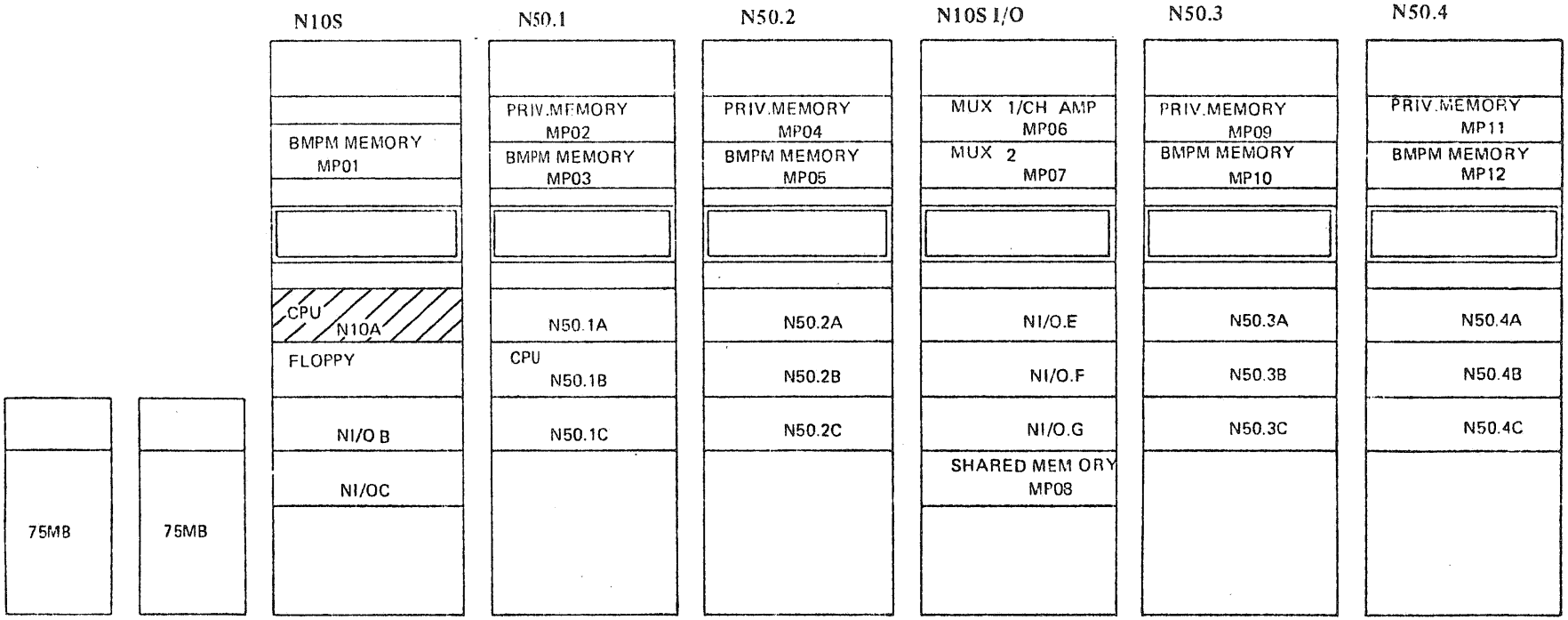
This chapter will deal with the CPU and LOCAL MEMORY card crate located in the NORD-10/S cabinet and named A.

The chapter starts with a overview where the main components described in Chapter 1 are located.

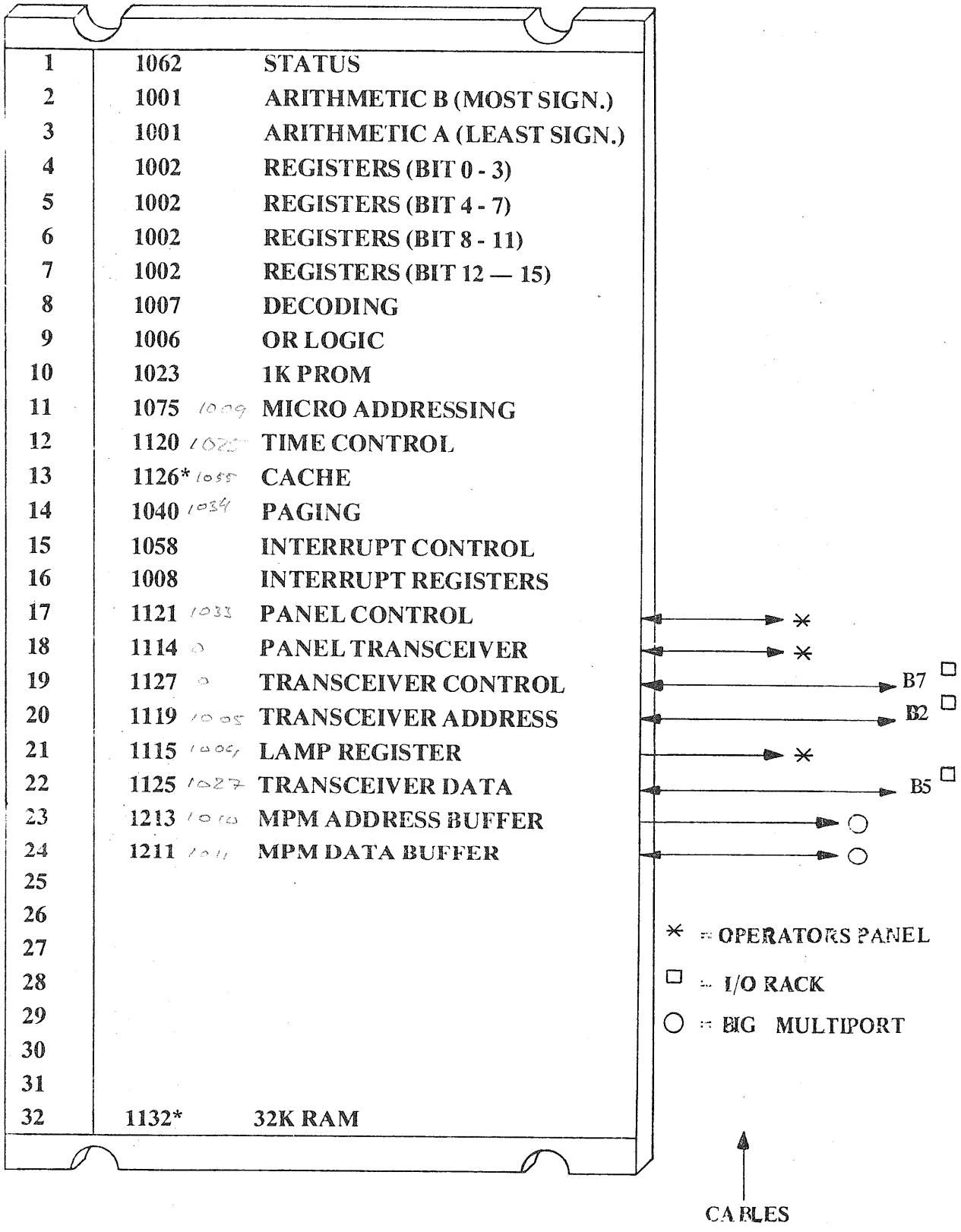
A brief description of the circuits found on each printed circuit board (PCB) follows.

A reference to where circuits are to be located on the module is given in the [ ] and also can be found in the hardware drawings.

SYSTEM CONFIGURATION F16



RACK A: NORD-10/S CPU AND LOCAL MEMORY



* = Option

2.1 *CPU AND LOCAL MEMORY OVERVIEW*

FUNCTION:	*ON PCB:*	*IN POSITION:*
CPU-REGISTERS: A,T,D,B,X,L,P (STS)	1002(1062)	A4,A5,A6,A7(A1)
ARITHMETIC	1001	A2,A3
ADDRESS-ARITHMETIC	1002	A4,A5,A6,A7
INSTRUCTION EXECUTE CONTROL LOGIC/TIMING	1075,1023 1007,1006 1062/1120	A11,A10 A8,A9 A1,A12
MEMORY MANAGEMENT SYSTEM	1040	A14
INTERRUPT SYSTEM	1008,1058	A16,A15
CACHE MEMORY	1126	A13
OPERATORS PANEL:		
CPU INTERFACE	1114,1115, 1121	A18,A21,A17
MAIN MEMORY:		
INTERFACE/DRIVER* FOR ADDRESS	1119/1213*	A20/A23*
INTERFACE/DRIVER*,RECEIVER FOR DATA	1125/1211*	A22/A24*
INTERFACE CONTROL	1127	A19
PARITY GENERATE/CHECK	1125	A22
*IF BIG MULTIPORT		
I/O SYSTEM:		
INTERFACE/DRIVER, RECEIVER FOR ADDRESS	1119	A20
INTERFACE/DRIVER, RECEIVER FOR DATA	1125	A22
INTERFACE CONTROL	1127	A19

2.2 *MODULE DESCRIPTION*

1062 — STATUS — POSITION A1

THIS PCB CONTAINS:

- Status Register (STS) Bit 0-7 on 16 Levels (PM,TG,K,Z,Q,O,C,M) [19A,16A]
- Overflow Detection [4D]
- Floating-Rounding Detection (TG) [13C,7C,10C]
- Carry-Generate For CPU ALU (74181) [1D,1B]
- Shift-Counter [7A,7B]
- Shift-Counter Zero Detection (TERM) [4A,10C]
- Circuits For Shift-Register Interconnection [19D,13D,16D,10D]
- Selector For Latching Discarded Shift-Bits (M-Flip-Flop) [7D]
- Signal True. Active When Tested Condition is Fulfilled [16C,19C]

1001 — MAIN ARITHMETIC B — POSITION A2 (Most Significant Arithmetic)

THIS PCB CONTAINS:

— The Arithmetic Logic Unit (ALU 74181) [314B-12/13B]

— ALU A-Operand Latch [15/16B,18/19B]

— ALU B-Operand Selector/Latch [1C-19C]

— ALU Carry-Look Ahead [1B]

— Bit-Mask-Encoder [6C,14C]

— ALU Result Latch (Sum-Bus Latch AC) [6D,10D,14D]

— 16 Bits Shift-Register [16/17D,3/4D]

THE MODULE IN POSITION A2 IS USED:

1. When *all* Instructions Are Executed.
   Instructions Using Arithmetic B (Most) and A (Least) are Given in the Next Page

2. When *all* Operators — Communication Commands are Executed. (In Stop Mode)

1001 – MAIN ARITHMETIC A – POSITION A3 (Least Significant Arithmetic)

IN THIS POSITION BOARD IS USED WHEN THE FOLLOWING INSTRUCTIONS ARE EXECUTED:

–	SAD		Shift A and D register
–	MIN		Memory Increment
–	NLZ		Integer → Floating
–	STB (LEFT)		Store byte
–	MPX 3		Multiply index
–	FAD		Add
–	FSB	Floating	Subtract
–	FMU		Multiply
–	FDIV		Divide
–	MPY	Integer	Multiply
–	DIV		Divide

1002 — REGISTERS POSITION A4 : BIT 0-3
A5 : BIT 4-7
A6 : BIT 8-11
A7 : BIT 12-15

THIS PCB CONTAINS:

— The Register Block (Programable)
Register: D,B,L,A,T,X and SP) [10D,-10C]

— The Scratch-Register (Microprogramable)
(Register: SSTS and SCR [12D,8C]

— The Current Program-Counter (CP) [12B]

— Address-Arithmetic [19A,18-19BC,1-2BC,1D]

— CPU Memory-Address Register (R = CPU Logical Address)
[10B]

— ALU A-Operand Selector [4-5CD-15-16BC]

— ALU B-Operand Pre-Selector [5E-15E]

— ALU Sum Selector [8B]

— H-Register (IB-Bus → CPU Reg. Block Latch)
[3A]

— H-Register, H-Register (Bit 0-7) With Sign Extension Selector [1A]

1007 – DECODING – POSITION A8

THIS PCB CONTAINS:

- Micro-Instruction Register Bit 19-31 [12C,14B]
- ALU Function Code Select Logic (SO-3,ARM) [10B,6B,4B,16B]
- ALU Input Carry Select [16B]
- Sum-Bus Designation Write (WD-WSSTS)
- CPU Double-Cycle Control Logic (Indirect, P-Reg = Designation) [16C,14C]
- Shift Register Function Control Logic (BSHS = Most, ASHS = Least) [4C,6C,8C]
- Latch-Pulse to Status Register Bit 0-7 (SKL) [19D]
- Register Block Level Select Signal (LSEL) [2B]
- CPU Address-Register Parallel Load Signal (RLD) [18B]

1006 – OR LOGIC – POSITION A9

THIS PCB CONTAINS:

- Micro-Instruction Register Bit 0-15 [5C-7C]
- Control Logic to Select Input to MIR 0-15 Either From:

  1. Instruction Register IRO-10
     OR
  2. Read Only Memory ROM 0-15
     [11B,13B (MIR 0-3), 15B,17B (MIR 4-6)
     13D,11D (MIR 8-11), 9A,9B (MIR 12-15)]

- Register Block, Paging Control Register Level Select (LEV0-LEV3) [5D]
- Address Arithmetic Control Signal (BRXAD) [15B]
- Alternative ALU-Function Select Signal (ALT Signal Active When: LDB,STB (Left Byte) NLZ, Floating, MPY, DIV) [3C]

1023 – 1KPROM – POSITION A10

1167 – 4KPROM – POSITION A10

THIS PCB CONTAINS:

– Read Only Memory Bit 0-31

– ROM Out of Range (Illegal Instruction) Detect Logic

– ROM Data Ready (ROMDRY) Signal Generator

1023 = One Shots
1167 = Delay Lines

1075 — MICROADDRESSING — POSITION A11

THIS PCB CONTAINS:

— Instruction Register (IR0-15) [2D-5A]

— Read-Only Memory Entry Point Selector From 4 Sources: (10B-12A)

1. Instruction Register Function Code Bits (IR15-11)
   (Instructions without sub-instruction field) EP = 2 (IR15-11) + 100_8

2. Entry Point for Instruction With Sub-Instruction Field

3. Entry Point for Micro-Program Sub-Instruction Return Jump
   (CAR 0-11)

4. Entry Point for Micro-Instruction Jump (MIR 0-11)

— Logic For Special Entry-Points:
(Interrupt, Panel Interrupt) [15C,18A,18B]

— Micro-Program Counter (MPC 0-11) [5B-8A]

— CPU Address Arithmetic Control Logic (SIR9,BREN,REL)

— Paging System Page Table or Alternative Page Table Select Logic [10C]

1120 — TIME CONTROL = POSITION A12

THIS PCB CONTAINS:

— Main Oscillator (Delay-Line, 65ms) [2E,4E]

— Logic For Stopping the Main-Oscillator, [8D,6E,4D,2B]
Active During:
*Indirect Addressing, *Waiting, for Main-Memory, *Waiting for Read Only Memory

— CPU Main State Flip-Flops/Control Logic/Decoding
(LTC0-LTC2/RET3,RET7/T0-T5)

— Micro-Instruction Execute Control Logic (AAKL,BAKL,ACKL,BCKL,NJMP)

— Main Memory Communication Logic (Fetch,Find,Write) (IDRY,CIKL,HKL)

— Read Only Memory Communication Logic (ROMRQ,MRDRY,MIRKL)

— Registers Outside the Register Block Decoding/Communication Logic
[14A,11-12A]/(TRR,TRA,AEN)

— Paging System Page Protection Control Logic [16A]

1040 — PAGING — POSITION A14

THIS PCB CONTAINS:

- The Page Index Tables (Shadow Memory) (Static Memory 16 Bits Wide, 4x64 Words With Logical ADR: 177400-177777) [1A-5E]
- Logic For Selecting One of the Four Page Index-Tables (TS0, TS1) [13B, 13C]
- The Paging Control Register (PCR) on 16 Levels [15B = Ring, 13A = Level, 13B = Table Select]
- The Paging Status Register (PGS) [9D = Page Number, 11D = Page Table, Permit Violation/ Ring Violation Interrupt]
- Written in Page and Page Used Detect Logic [1A, 19A/1B]
- Circuit For Ring-Protection [16D]
- Shadow-Memory Address-Range Detect Circuits (Shadow) [11B]
- Memory Bank-Register (ADR Bit 16 and 17) [15C]

1058 – INTERRUPT CONTROL – POSITION A15

THIS PCB CONTAINS:

- Internal Interrupt Detect Registers (ID1-ID10) [13D-5D]
- Internal Interrupt Enable Registers (IE1-IE10) 15C,7C]
- Internal Interrupt Priority Decoder [9D,11D]
- Miscellaneous Register [ID] Used by Microprogram to Execute:

  ION, IOF (Interrupt System On, Off)
  PON, POF (Paging System On, Off)
  MON, Monitor Call

- MOPC Flip-Flop. (CPU in Stop-Mode)
- Interrupt Synchronizer (Interrupt When Instruction Fetch) [7A]
- Immediate Internal Interrupt (Not Wait On Fetch) [19D,13A,11A,11B]
- Paging System:
  - Memory Protect Violation Detect [15B]
  - Paging Control Register Write Pulse [5A]
  - Paging Status Register Clock Pulse [13B,11B]

1008 – INTERRUPT REGISTERS – POSITION A16

THIS PCB CONTAINS:

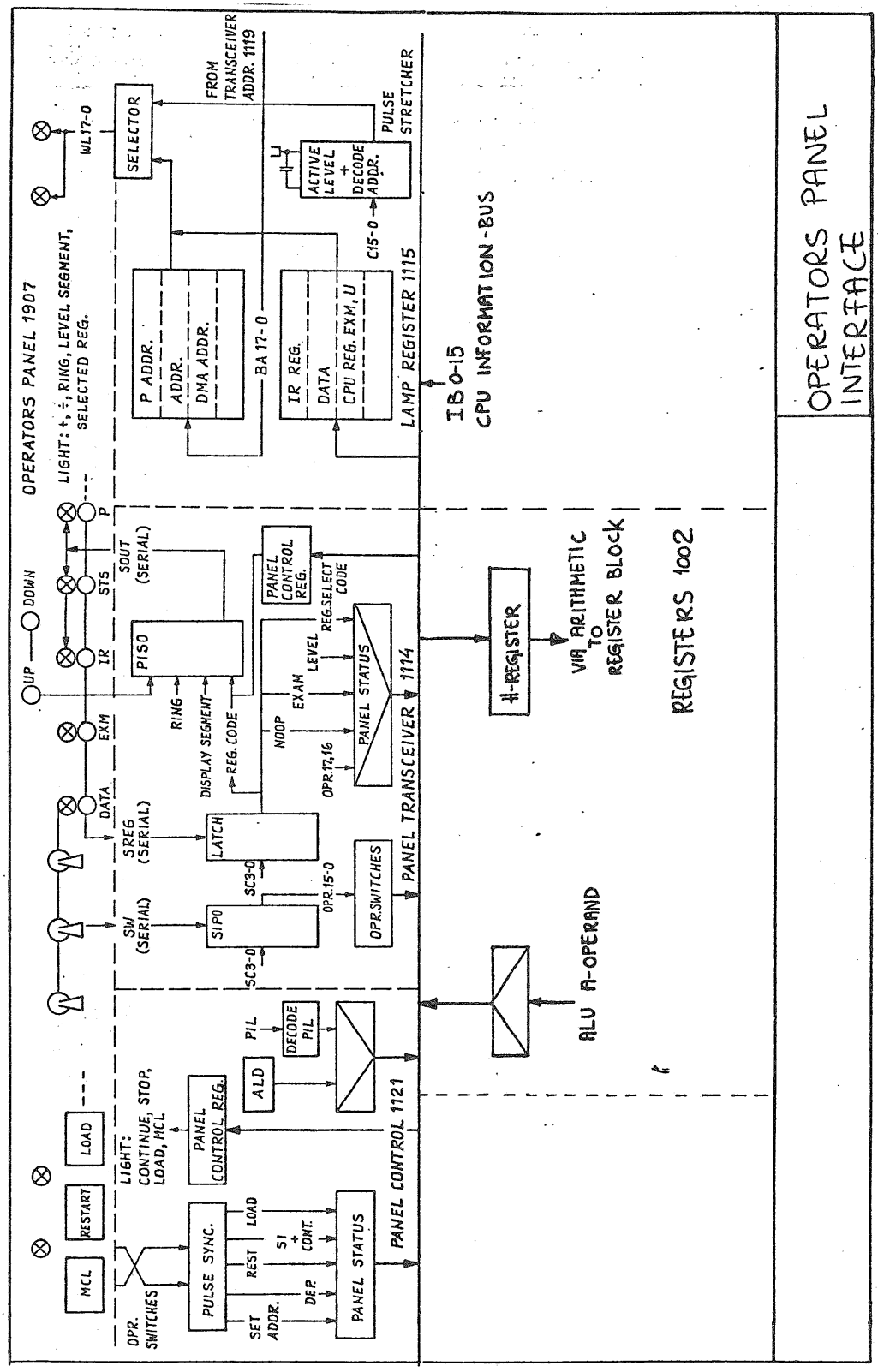
- Priority Interrupt Detect-Register (PID) [15E-6E]
- Priority Interrupt Enable Register (PIE) [18E-2E]
- Current Interrupt Level Register (PIL) [9A]
- Previous Interrupt Level Register (PVL) [13A]
- Highest Priority Interrupt Level Detect (PK) [7B,13B,9B]
- Highest Priority Interrupt Level and Current Level Compare (DIFF) [11B]
- Selectors Selecting One of Four Sources on to the IB-Bus [18C-2C]

    1. Internal-Interrupt Code
    2. PIE
    3. PID
    4. Previous Level (IRR PVL DP)

1121 – PANEL CONTROL – POSITION A17

THIS PCB CONTAINS:

- Automatic Load Descriptor (ALD) [1E-19E]
  (Gives Loading Device When Load-Button in Panel is Pushed)
- Decoded Current Interrupt Level (PIL) [10E,14D]
  (Active When Executing Wait Instruction With Interrupt System On)
- Panel Status Register (PAS) Bit 8-12 [12B]
  (Read and Examined by the Microprogram)
- Receiver Circuits for Signals From Panel Push-Buttons [16C,14A,16A]
- Signals to Light up Operators Panel Push-Buttons [8C,4A]
  (Set by Microprogram)
- Power Fail/Restart Control Logic [16C,10A,18A]



OPERATORS PANEL INTERFACE

1114 — PANEL TRANSCEIVER — POSITION A18

THIS PCB CONTAINS:

— Communication Logic for Serial Exchange of Data Between the Panel Board 1907 and the 1114 Board Each 2.5 ms

1114 → Panel (To Light Up Panel)

Signal SOUT Terminal 91 To Light:

1. + (Plus) — (Minus)
2. Paging Ring Number (RING 0-3)
3. Interrupt Level (DDO-3) (Segment Light)
4. Selected Register
   (Parallel Input Serial Output Register [4D,10B]

Panel → 1114 (Panel Information)

5. Operators Panel Switch Register (SW)
6. Panel Push-Buttons (SREG)
7. + (WUP) And — (WDOWN) Push-Buttons
   (Serial Input Parallel Output Register)
   [5B,2B,16B] = OPR (18 Bits)
   [4C] = Panel Push-Buttons Coded

— Panel Status Register (PAS) Bit 0-7 and 13-15
Read by Microprogram if Bit 13 = No Operation = 0

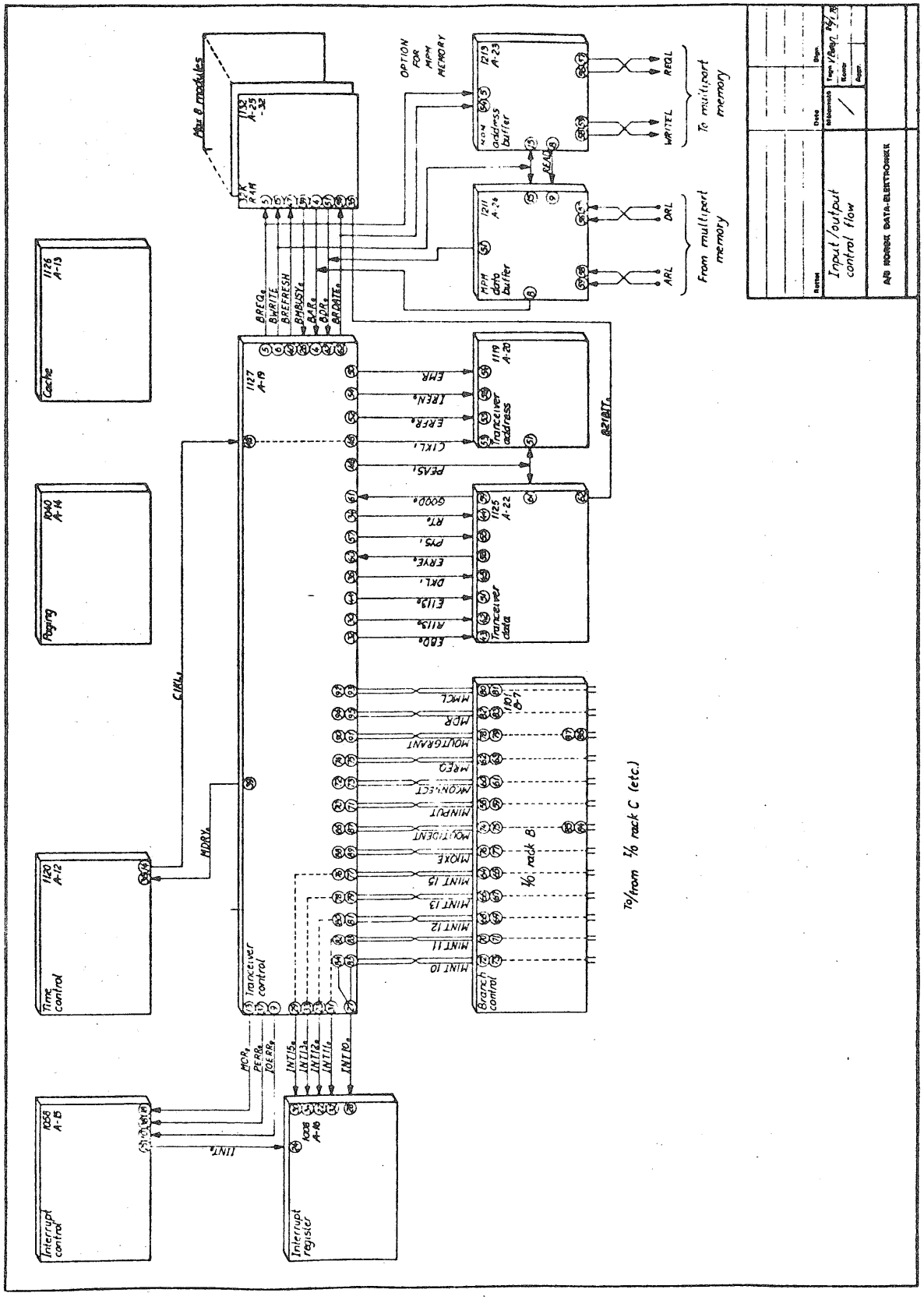
Bit 13 = 0 if One of the following buttons is pushed:

EXM,STS,P,L,B,X,T,A, or D

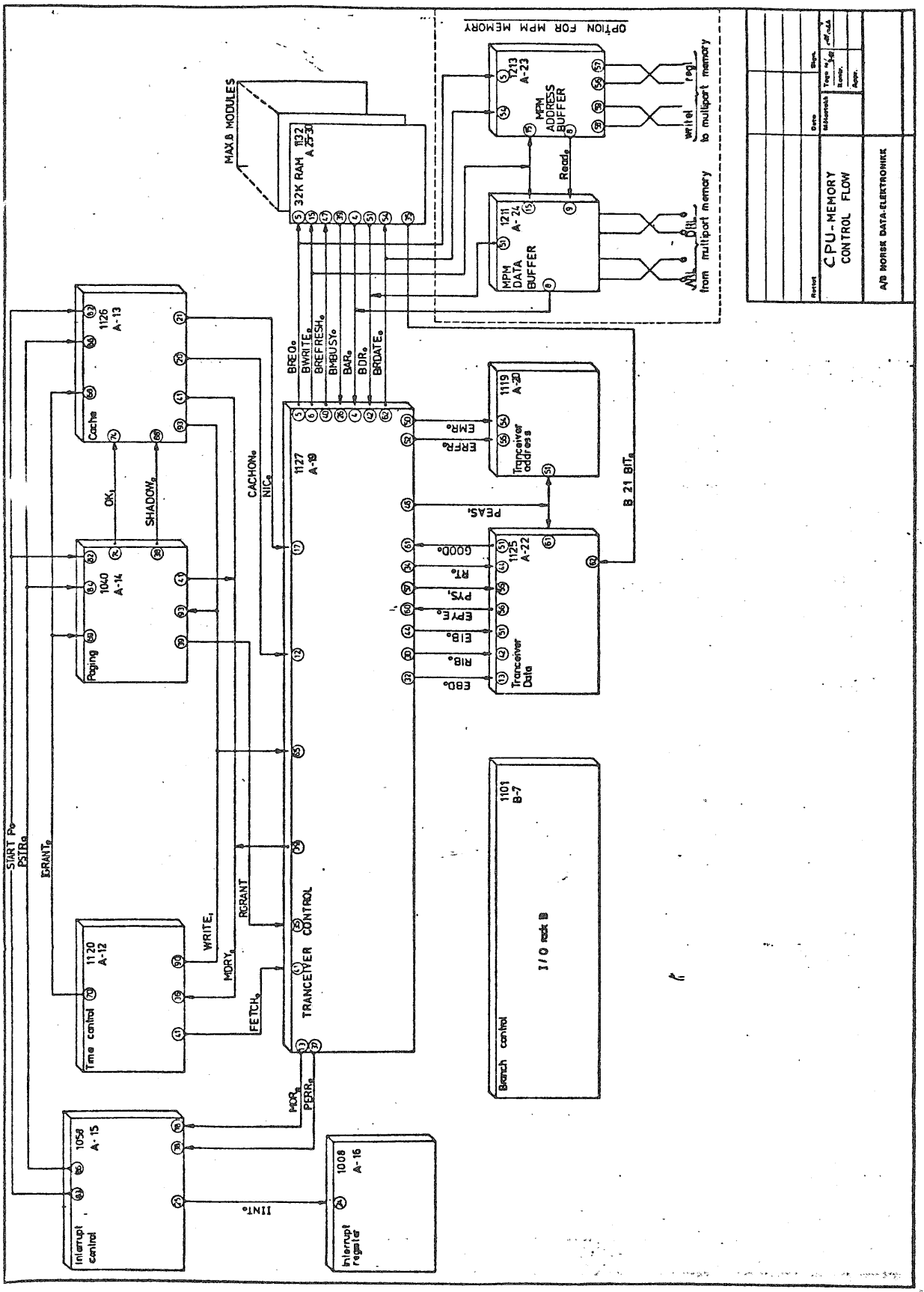
1127 – TRANSCEIVER CONTROL – POSITION A19

THIS PCB CONTAINS:

- Control Signals for Establishing the Communication Between:
  1. The CPU and the Input/Output System (B and C-Rack)
  2. The CPU and the Main Memory (Local and Multiport)
  3. The Input/Output System and the Main Memory During a DMA-transfer
- Drivers/Receivers/Control Logic for the Main Input/Output Bus Control Signals (Connected via A 1:1 Cable to the Board in Position B7)
- Main Memory Address Bus (BA) and Data Bus (BD) Allocation Network. Allocated According to this priority among the Sources:
  1. DMA
  2. Refresh (Local Memory)
  3. CPU
- Timeout Circuits (6μs) for the Memory (No Memory Data Ready) and the I/O System (No Connect)
- Parity Error Address Register (PEA) Bit 0-7



INPUT/OUTPUT CONTROL FLOW

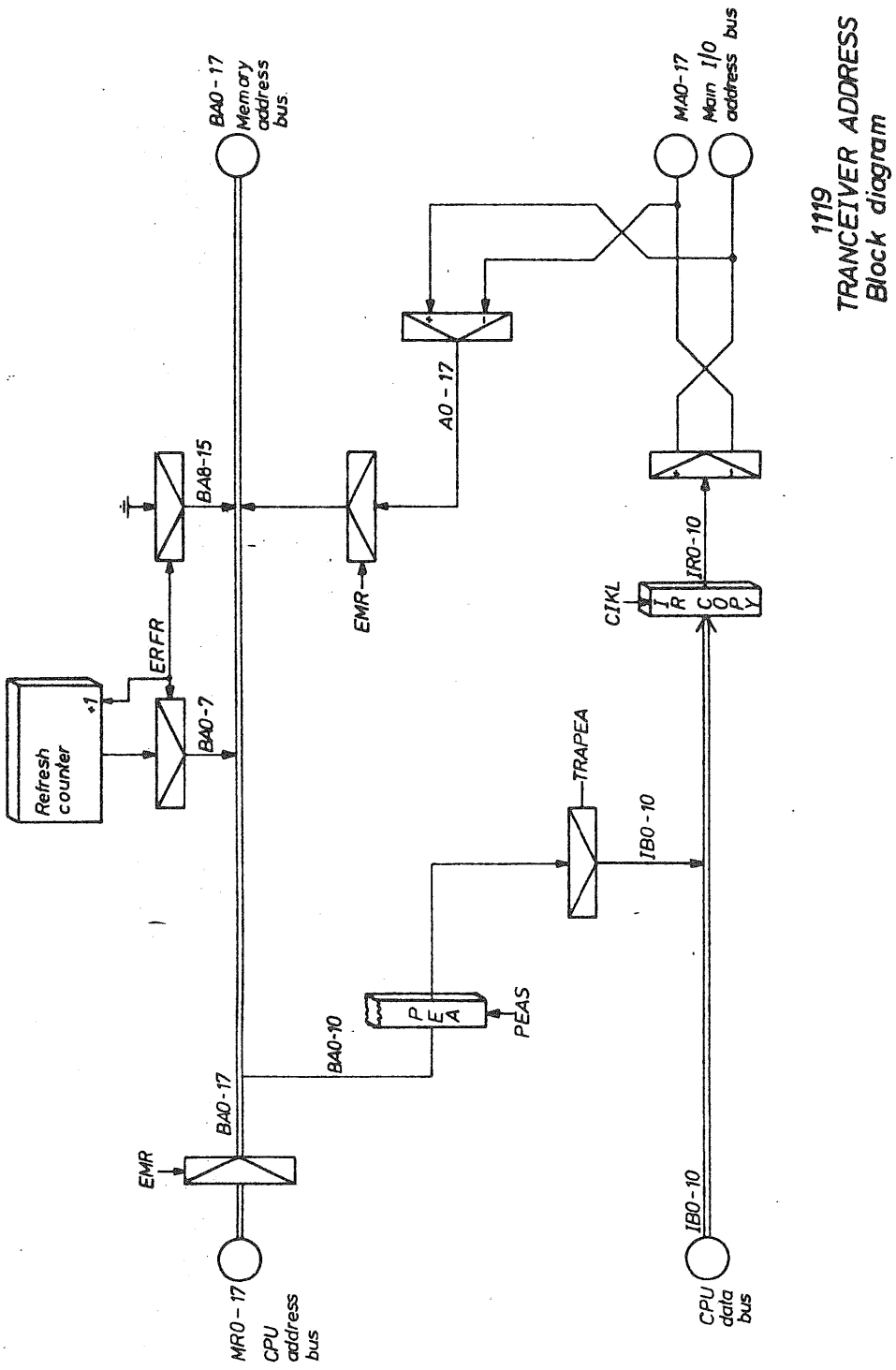


CPU-MEMORY CONTROL FLOW

1119 – TRANSCEIVER ADDRESS – POSITION A20

THIS PCB CONTAINS:

- Driver/Receiver Circuits for the Main Input/Output Address Bus [11A,11B-11C]
- Instruction Register Copy (IR 0-10) (In Use While Executing an IOX or IDENT Instruction) [3C,1C]
- Circuits for Enabling the CPU Address (MR 0-17 From Paging) Onto the Main Memory Address Bus (BA 0-17) [5A,7A,9A]
- Circuits for Enabling the Main I/O Address Bus (MA 0-17) Onto the Main Memory Address Bus (BA 0-17) During a DMA via the CPU. (If Position 8 in the B-Rack is Empty) [11D,19D,15D]
- Local Memory Refresh Oscillator/Driver [3D/5D,7D,9D]
- The 11 Lower Bits of the Parity Error Address Register (PEA) [5B,7B]



1119 - TRANSCEIVER ADDRESS
Block Diagram

1115 – LAMP REGISTER – POSITION A21

THIS PCB CONTAINS:

– Three 18 Bits Registers Where the Main Memory Address Bus BA is Latched as Follows:

Reg:	*Latched:*
1:	During Instruction Fetch
2:	During Memory Operand Read/Write
3:	During DMA-Transfer To/From Local Memory [2A-10A]

(Register 1 is Selected to the OPR Panel (WLO-WL17) when the PADDR Button is Pushed

Register 2 when the ADDR Button is Pushed
and
Register 3 when the DMA ADDR Button is Pushed)

– Three 16 Bits Registers Where the CPU IB-Bus is Latched as Follows:

Reg:	*Latched:*
1:	When an Instruction on the IB-Bus
2:	When Data on the IB-Bus
3:	When the Microprogram Writes into it or an TRR OPR Instruction is Executed

(Register 1 is Selected When IR is Pushed
Register 2 is Selected When DATA is Pushed
Register 3 is Selected When STS,P,L,B,X,A,D,EXM or U is Pushed)

– Pulse Stretcher [18D-12C] Active When Either:

1: Active Level is Pushed
or
2: Decode Address is Pushed

– Address (BA12-15) and Active Level (PL0-PL3) Decoder [10D,10C]

1125 — TRANSCEIVER DATA — POSITION A22

THIS PCB CONTAINS:

— Circuits to Enable the Main I/O Data Bus (MO-15) Onto the CPU IB-Bus and Vice Versa
(During IOX and IDENT) [3A-7A,13E-19F,15A-19A]

— Circuits to Enable the CPU IB-Bus Onto the Main Memory Data-Bus BD and Vice Versa
(During CPU Fetch, Read and Write) [3A-7A,1A-5A]

— Circuits for Control Code Bits (Parity Bits) Generation During Memory Write (C5-C0) (C0-C4 if 21 Bits Local Memory) (C4 and C5 if Multiport Memory)

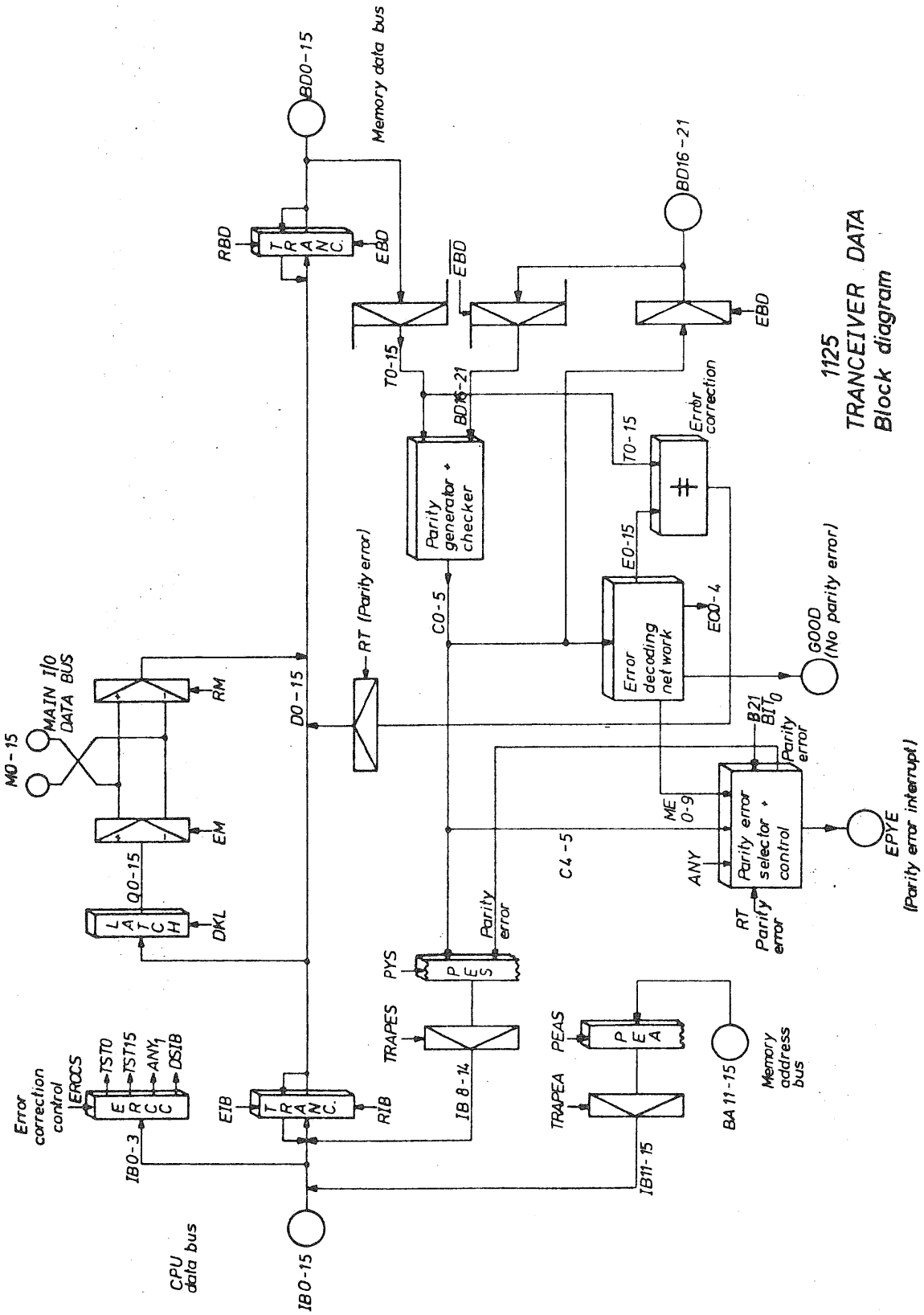
— Circuits for Error Checking/Correction During Memory Read.
[3G-1G,3D-9D/3E-7C,1D-17F]
Corrects Single Error
Detects Muliple Error

— Circuits for Error Reporting [11D,17E,15G,17G]
Internal Interrupt to Level 14
Multiple error Gives Always Interrupt
Single Error Gives Interrupt if ERCC REG 2 = 1 (Any-Bit)

— Error Correction Control Reg (ERCC) [IF]

— Parity Error Status Register (PES) Bit 9-14 = C0-C5

— Parity Error Address Register (PEA) Bit 11-15



1125 — TRANSCEIVER DATA
Block Diagram

1213 – MPM ADDRESS BUFFER – POSITION A23

NB! This Board is not Used in Configuration With Only Local Memory

THIS PCB CONTAINS

- Address Drivers for the CPU and DMA Address to Multiport Memory (BAOL-BA17L)
- Multiport Memory Address Range Limit Switches (Upper and Lower) Active in Configuration With Both Multiport and Local Memory [5D]
- Address Range Against Switch Setting Compare Circuits [7C,5C = Lower Limit, 7B,5B = Upper Limit]
- Multiport Memory Control Signal Drivers (Request and Write) Active if Address Within Limit (ADD ok)

1211 – MPM DATA BUFFER – POSITION A24

NB! This Board is not Used in Configuration With Only Local Memory.

THIS PCB CONTAINS:

- Data Drivers/Receivers for the CPU and DMA Data To/From Multiport Memory (BDOL-BD17L)
- Multiport Memory Control Signals Receivers (Data Ready; DR, Address Ready; AR)
- Enabling of Data Lines Control Logic (Data Lines Enabled Only When Address Within Limits on 1213 Board)

NORSK DATA A.S
Postboks 4, Lindeberg gård
Oslo 10, Norway

COMMENT AND EVALUATION SHEET

NORD-10/S General Description
October 1978

ND-06.013.01

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM _____

_____

_____