

Hewlett-Packard 9830 Computer Schematic

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Section: Title & Contents

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NOTE

This schematic has been derived through examination of the equipment. This is not the manufacturer's schematic.

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NOTES

- Printed circuit boards are identified by the Assembly Number printed in the foil of the circuit board. The last two digits of the assembly number distinguish each board type, and correspond to the color coding of the board extraction handles.

- This schematic presents the 4KW RAM board-set so the assemblies are identified as 82,83,84. The connectors they plug into remain identified as N22,N23,N24, from the original design for 2KW RAM boards.


- IC locations are identified by a label of the form:

U <assembly-type> - <enumeration>

or

U <assembly-type> - <row-alpha> <column-number>

A few boards have the IC locations in the foil, these are used for the enumeration if present. For the CPU and tape drive boards the same enumeration as presented in the HP patent and service manual is used. For other boards, a row-column locator is used, with the row specified by a,b,c,... and the column by 1,2,3,... starting at the upper left corner.

- The symbol  represents a connector pin. The solid black end is the male side, the white-filled end is the female side. Connector pins are identified by a label of the form: N <assembly-type> . <pin>
- A small black rectangular marker on the upper half of a gate symbol indicates an open-collector output.
- Capacitance in microfarads unless otherwise noted.

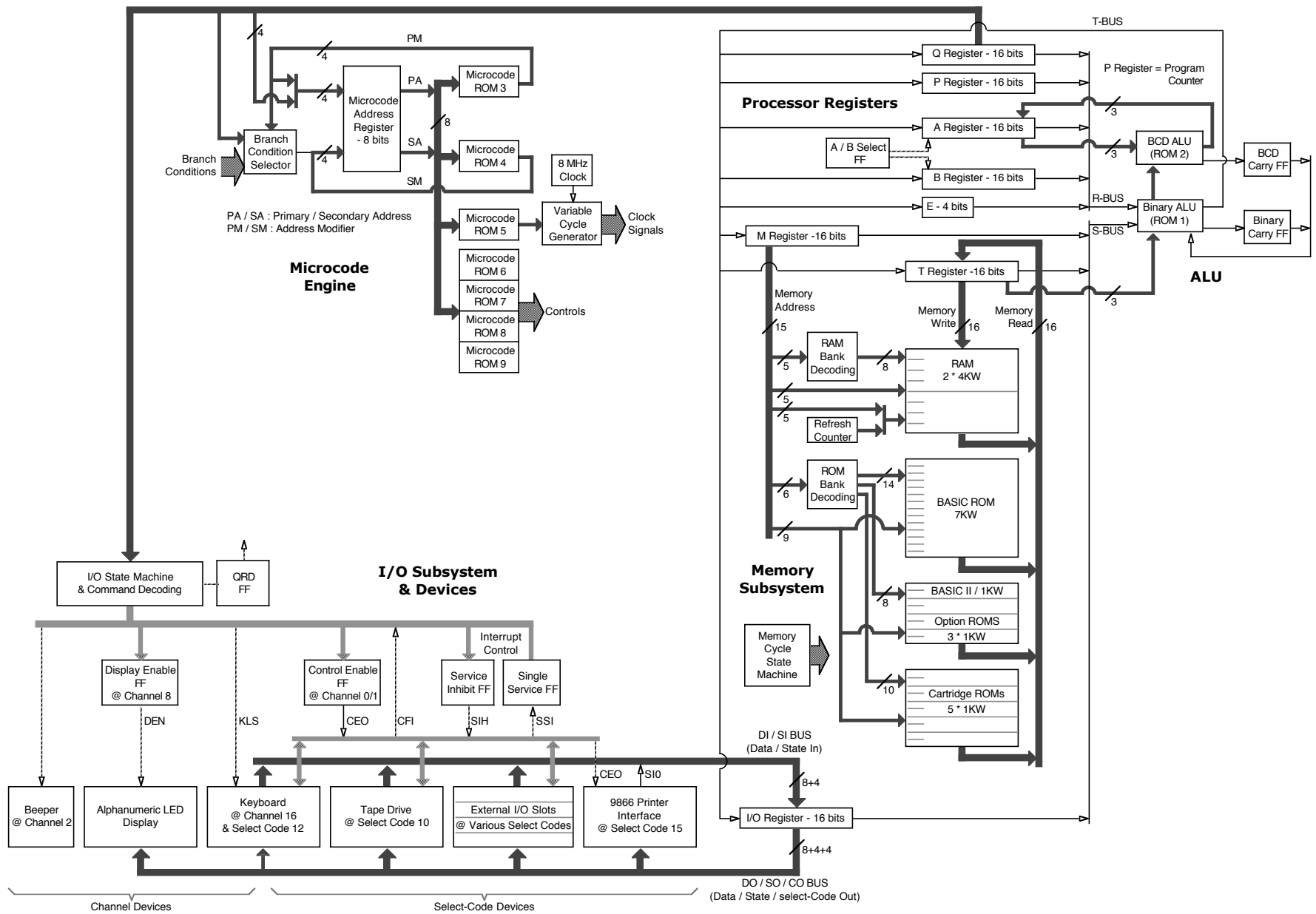
- This schematic is based on a reverse engineering of the 9830 board assemblies listed in the accompanying table, along with some use of the 9830 patent (US #4,012,725) and the tape drive schematics available in the the 9830 service manual.

- 2013 Spring: Drawn by bhilpert.
- 2013 Sep: Version 1

TO DO

- Add board layout for keyboard logic and tape transport, head.

Assembly Name	A #	Unit 1303A00748				Busted 'A' Remnants			
		RE USE	Foil # REV	Comp Date	Stamp Date	RE USE	Foil # REV	Comp Date	Stamp Date
Backplane	1	* •	09830-66501 REV B	-	APR 09 1973	-	-	-	-
External I/O Bus	2	* •	09830-66502 REV C	7305	APR 13 1973	09830-66502 REV C	7523	-	-
ROM Cartridge Bus	3	* •	09830-66503 REV B	7312	APR 16 1973	09830-66503 REV C	7528	-	-
CPU I/O	11		np	-	-	* • 09810-66511 REV B	7540	-	-
CPU Clock & I/O	12		np	-	-	* • 09810-66512 REV C	7528	-	-
CPU Microcode Engine	13		np	-	-	* • 09810-66513 REV A	7536	-	-
CPU Registers & ALU	14		np	-	-	* • 09810-66514 REV A	7539	-	-
BASIC ROM	21		np	-	-	* • 9830-66521 REV A	7406	-	-
M Register	82		np	-	-	* • 09830-66582 REV B	7419	-	-
T Register	83		np	-	-	* • 09830-66583 REV A	7313	JUN 05 1973	-
4KW RAM	84		np	-	-	• 5020-8304 REV A	7419	-	-
"	84		np	-	-	* • 5020-8304 REV A	7325	MAY 24 1973	-
ROM Buffer	25	* •	09830-66525 REV A	7312	MAR 30 1973	09830-66525 REV B	7536	-	-
ROM Card	26		np	-	-	* • 5020-6884 REV A	7532	-	-
Keyboard Matrix	31	* •	09830-66531 REV B	-	-	• 09830-66531 REV B	-	-	-
Keyboard Encoder	32	* •	09830-66532 REV D	7649	-	09830-66532 REV D	7537	-	-
Keyboard Interconnect	34	* •	09830-26534 REV B	-	-	09830-26534 REV B	-	-	-
Display	41	* •	09830-66541 REV D	7452	-	09830-69541 REV E	7511	-	-
Display Logic	42	* •	09830-66542 REV A	7308	MAR 30 1973	np	-	-	-
Power Supply	51		09830-66551 REV A	7308	-	* • 09830-66551 REV A	7526	-	-
Tape Interface	61	* M •	09830-66561 -	7307	APR 17 1973	09830-66561	7531	-	-
Tape Control	62	* M •	09865-66562 REV B	7309	MAR 24 1973	np	-	-	-
Tape R/W	63	* M •	09865-66563 REV C	7313	APR 11 1973	09865-66563 REV D	7408	DEC 12 1973	-
Tape Motor Control	64	* M •	09865-66564 REV B	7311	APR 24 1973	np	-	-	-
Tape Interconnect	65	* •	09830-66565 REV B	7405	JAN 17 1974	np	-	-	-
Tape Head Amp	66	* •	09865-66566 REV B	7349	-	np	-	-	-

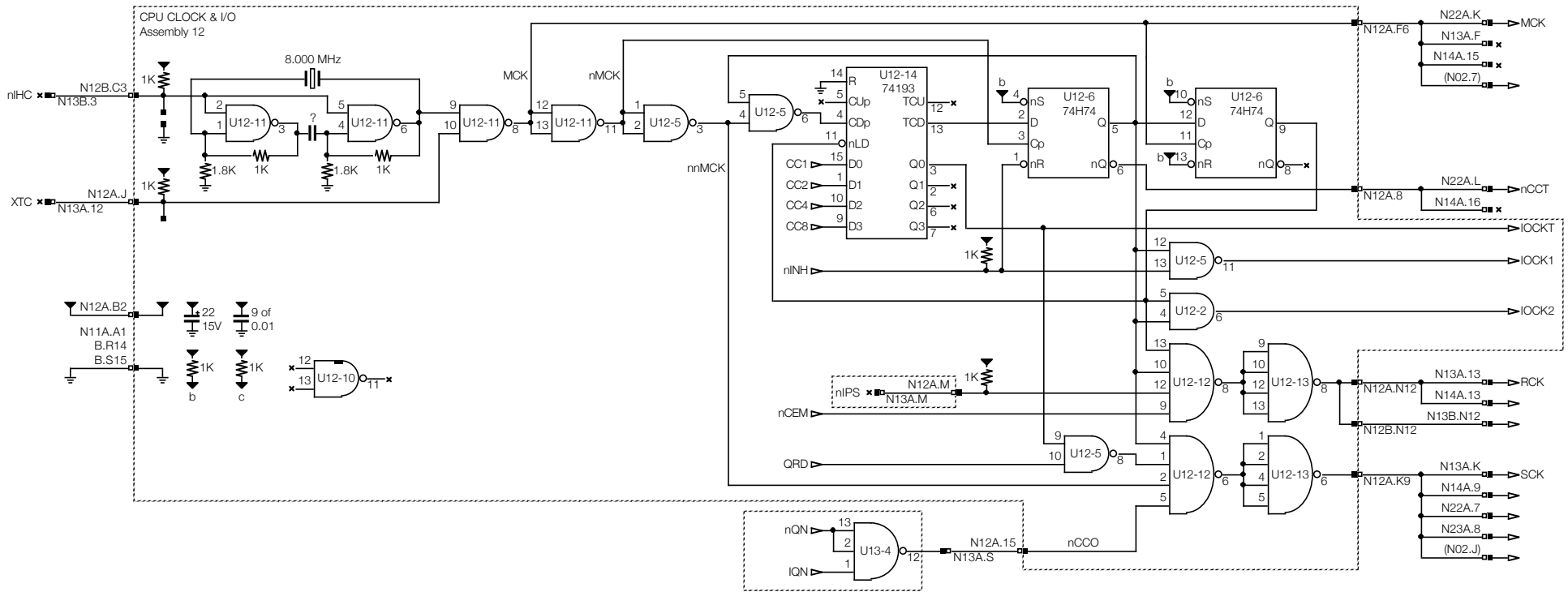


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Section: Block Diagram

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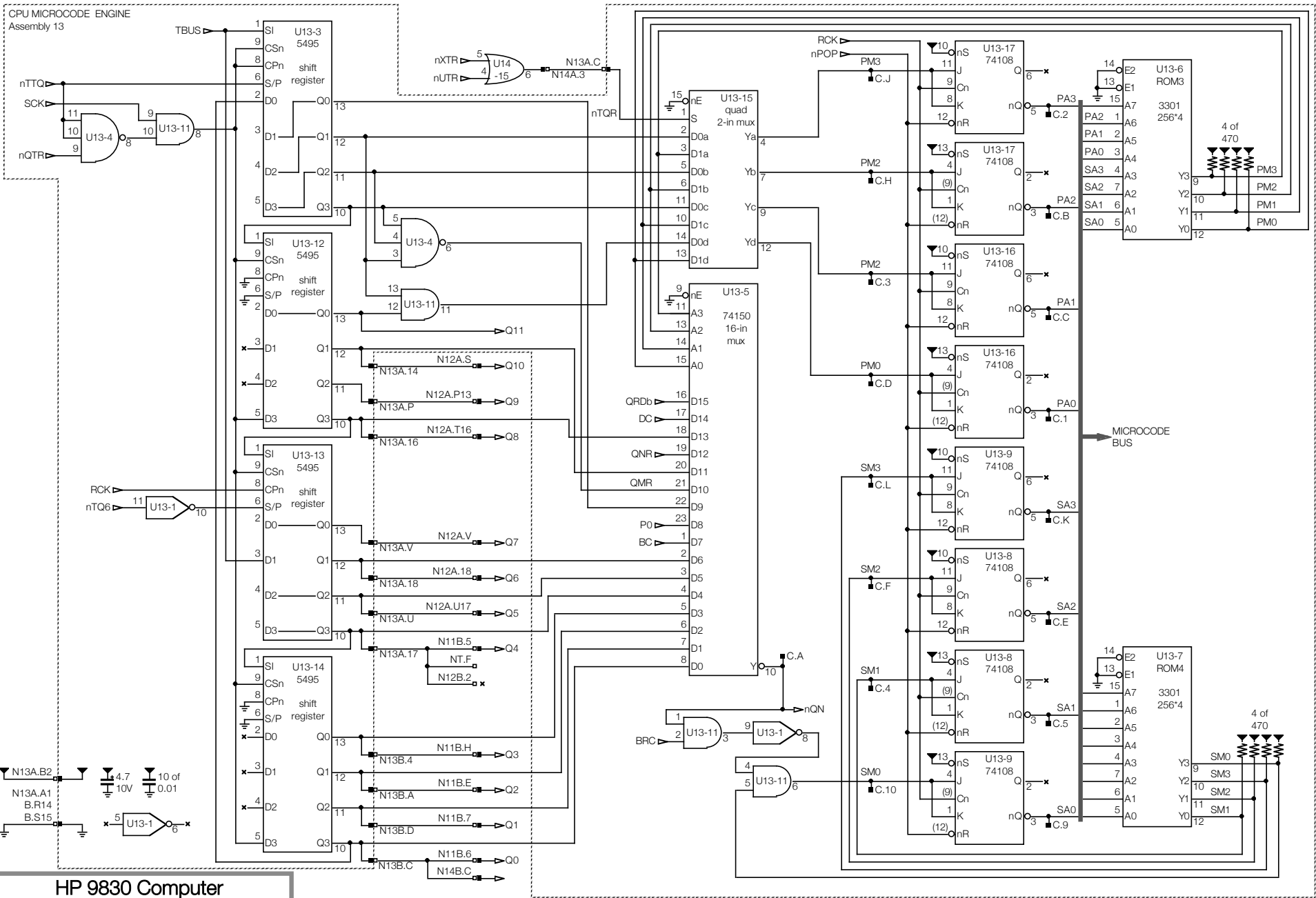


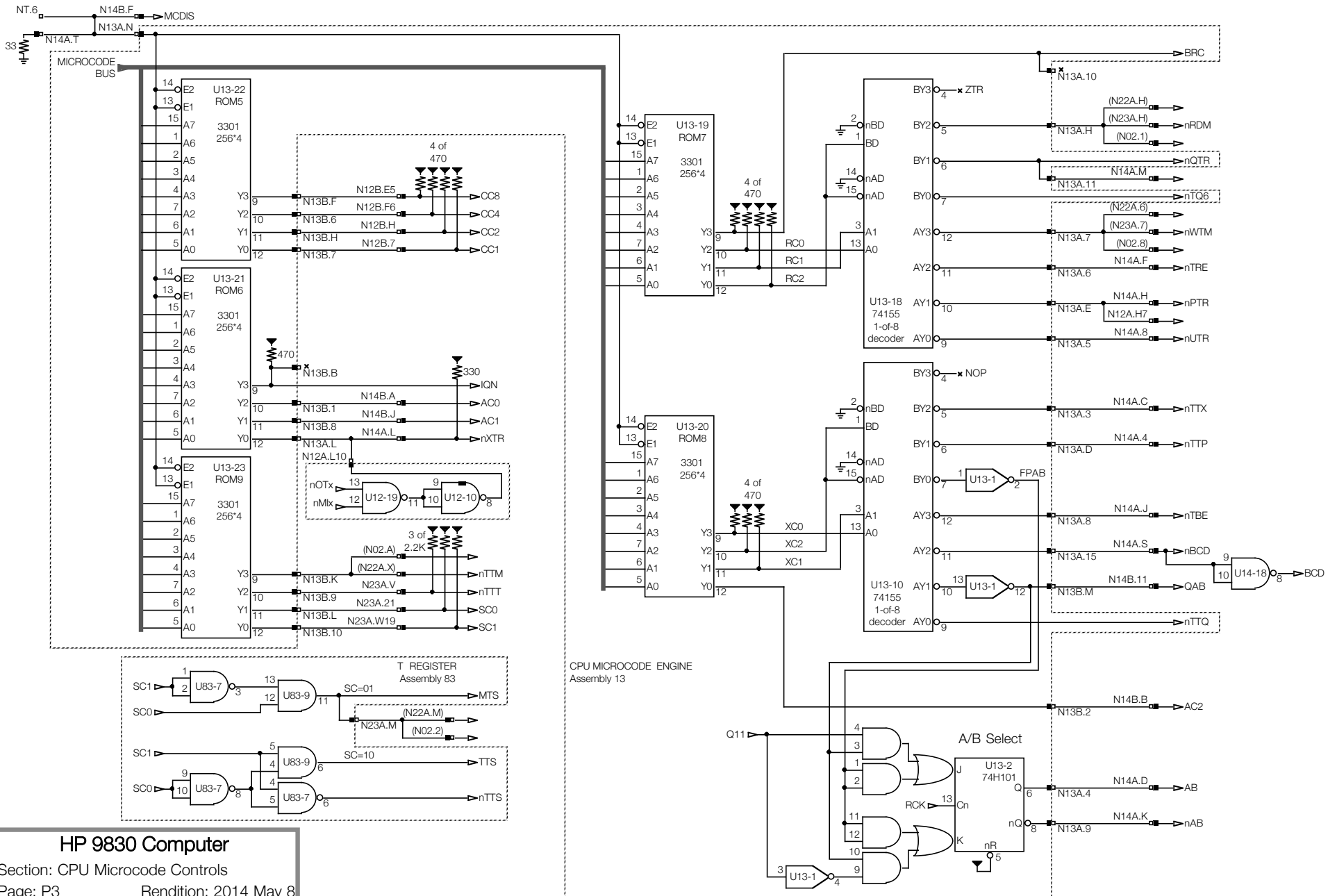
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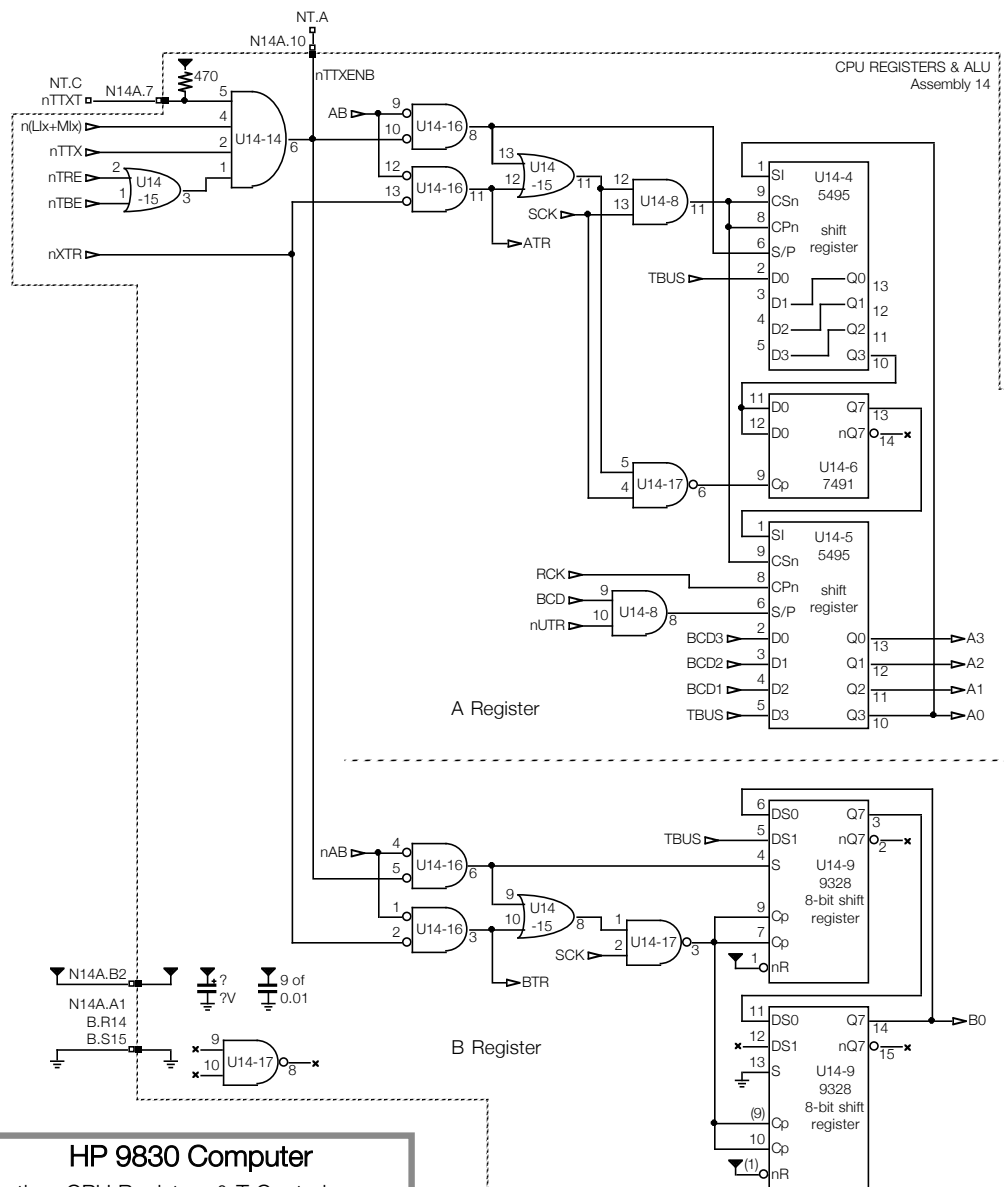
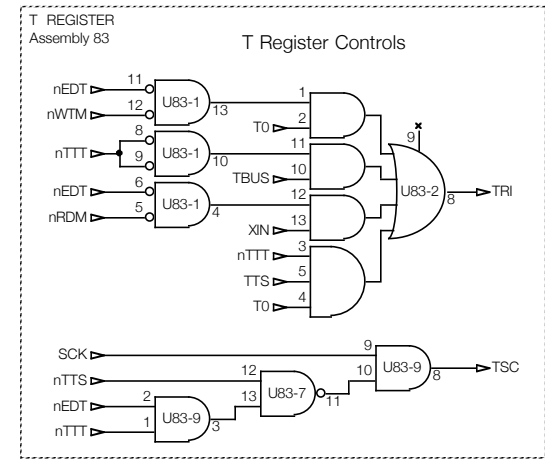
Section: CPU Clock

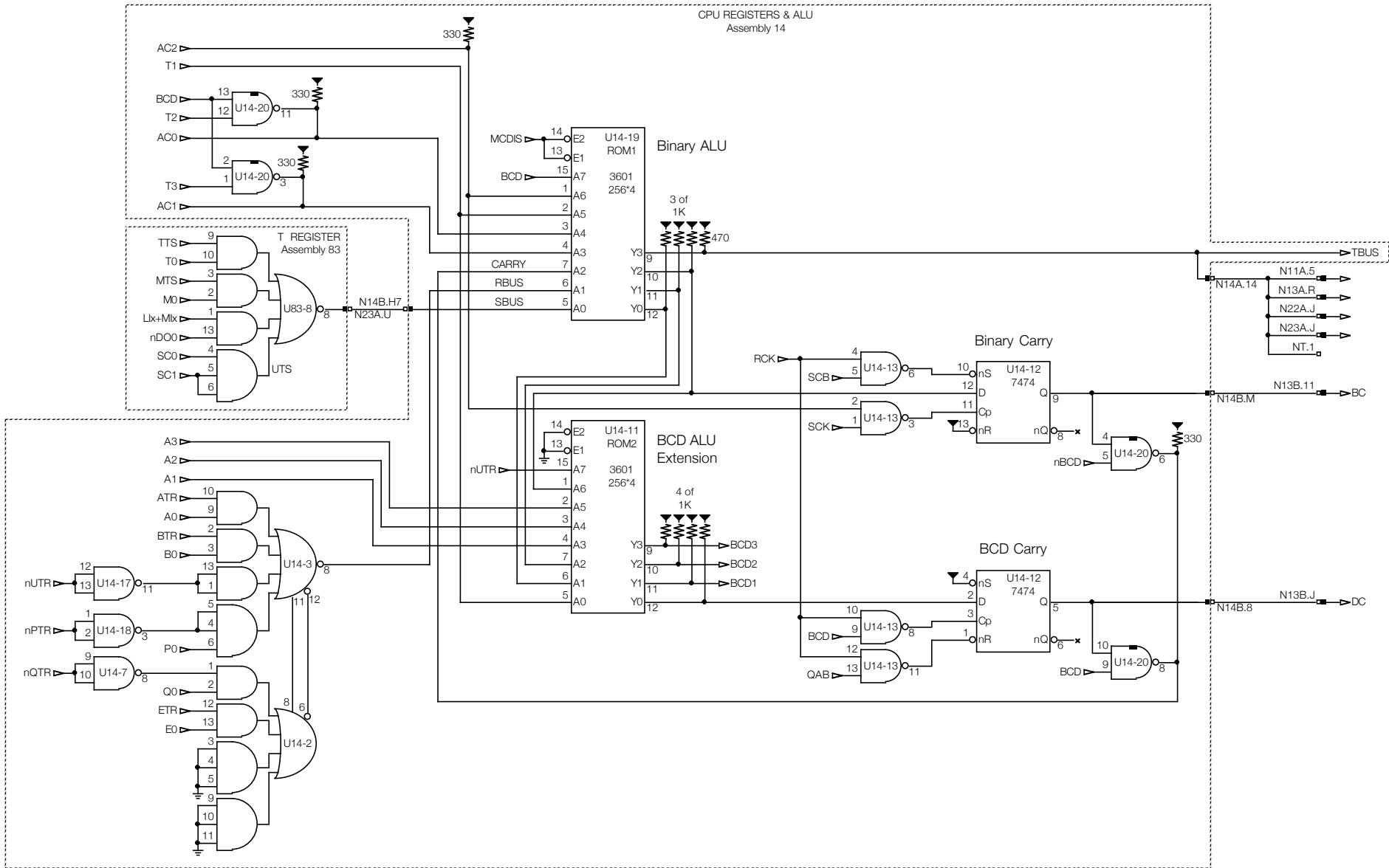
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Section: CPU ALU

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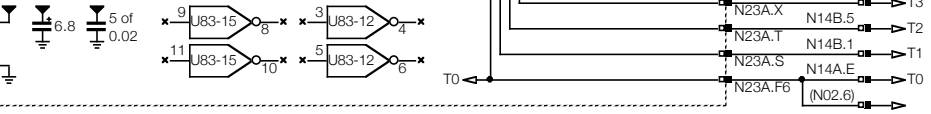
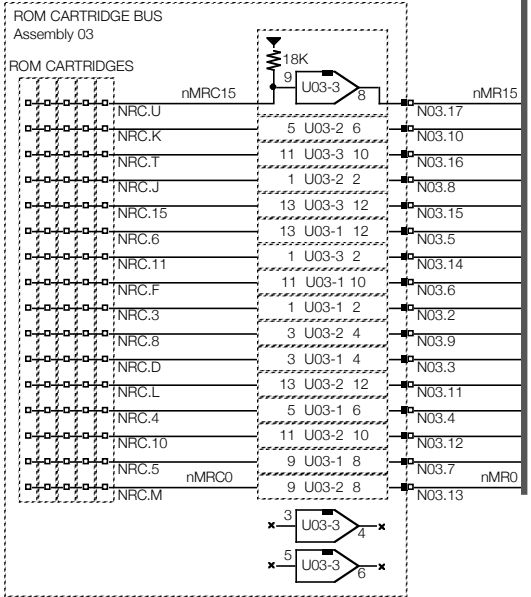
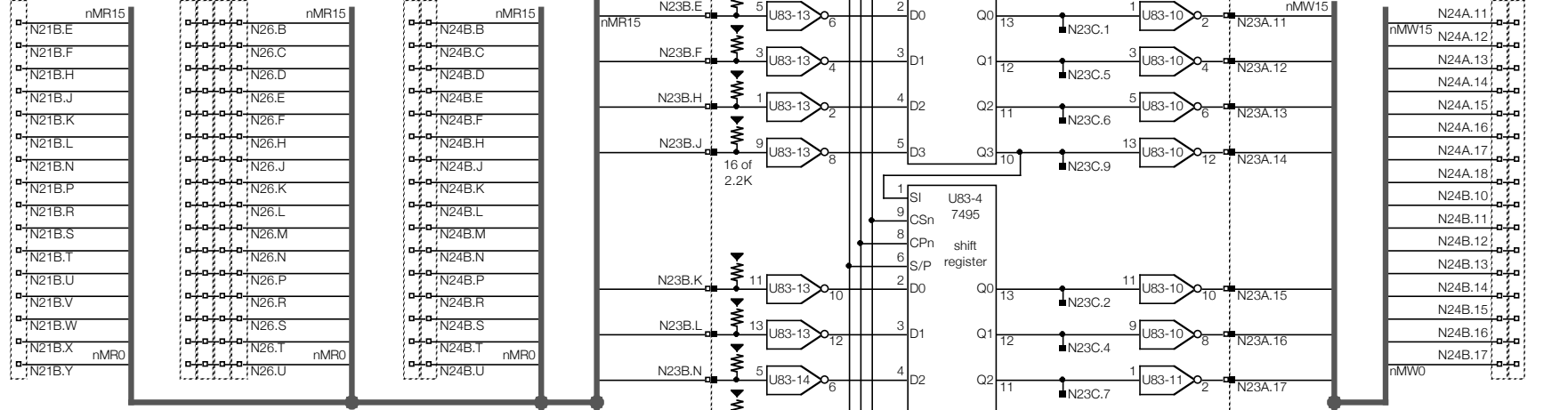
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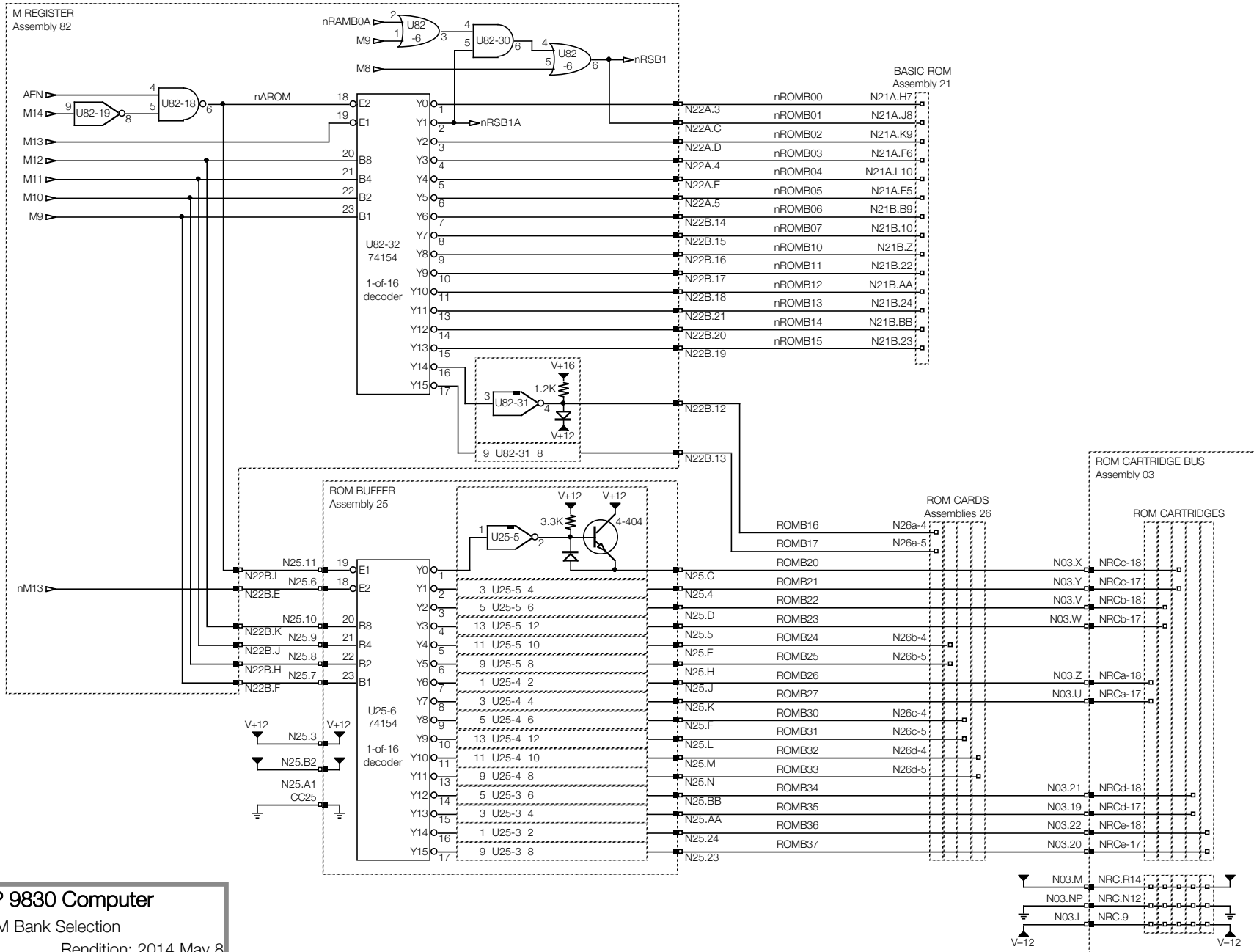
BASIC ROM
Assembly 21

ROM CARDS
Assemblies 26

4KW RAM
Assemblies 84

4KW RAM
Assemblies 84



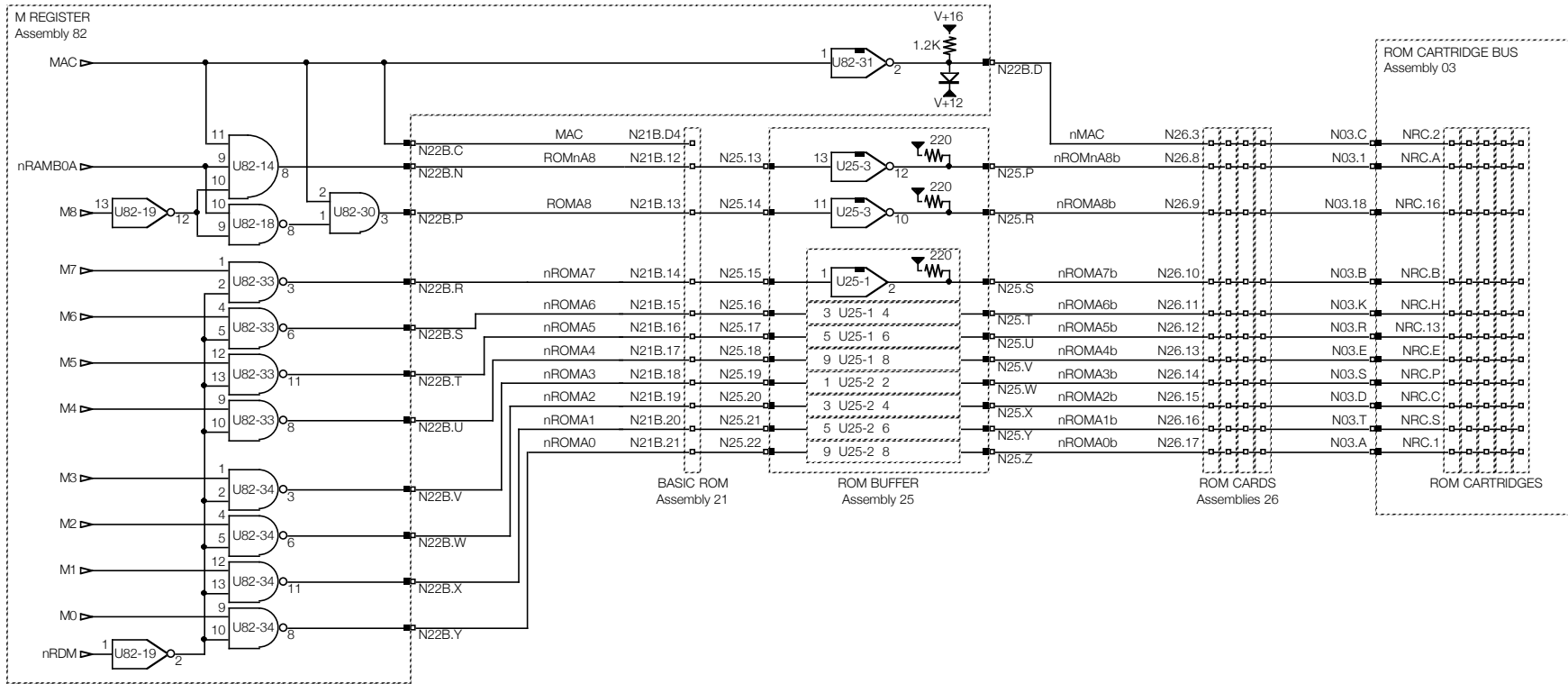


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Section: ROM Bank Selection

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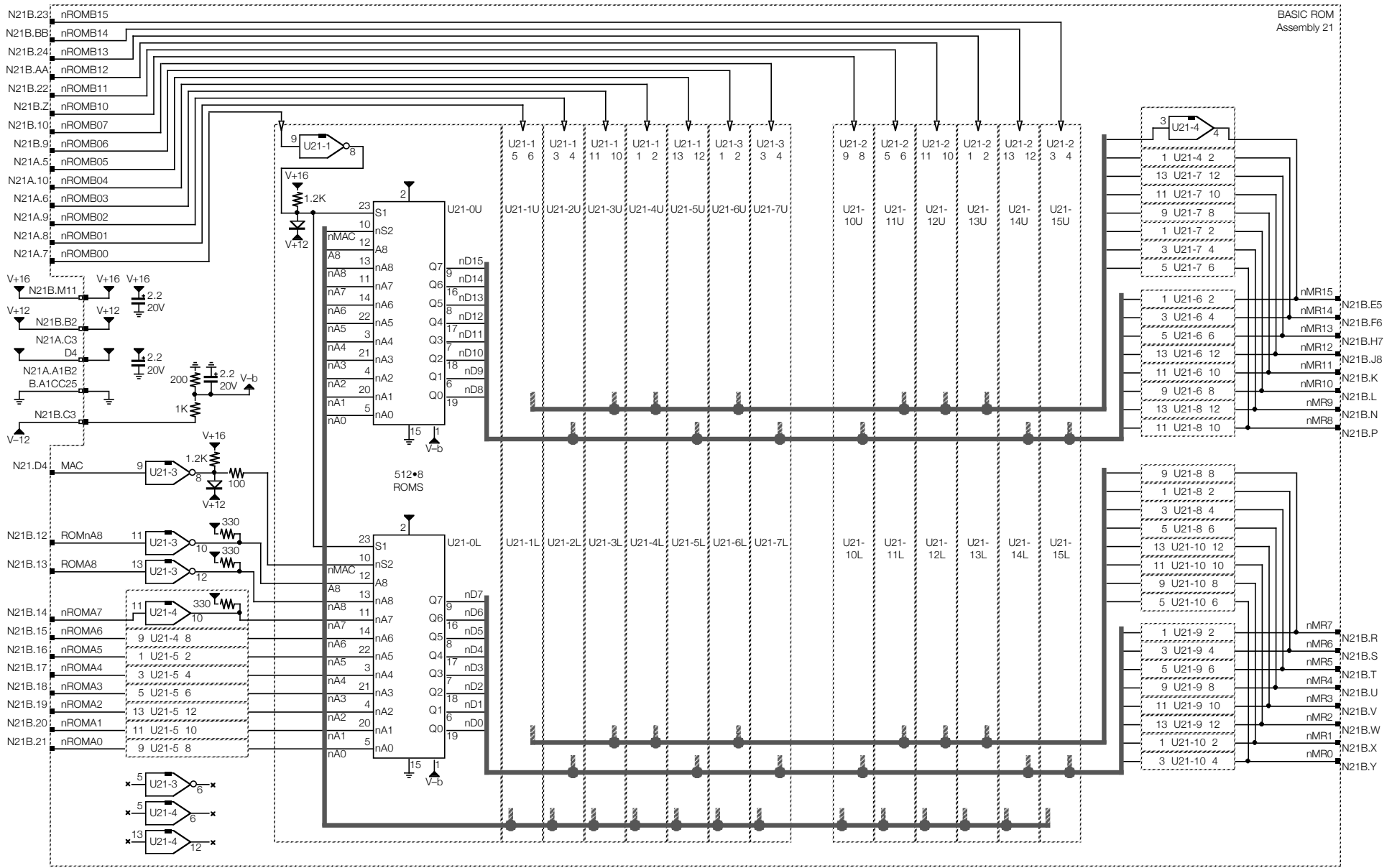


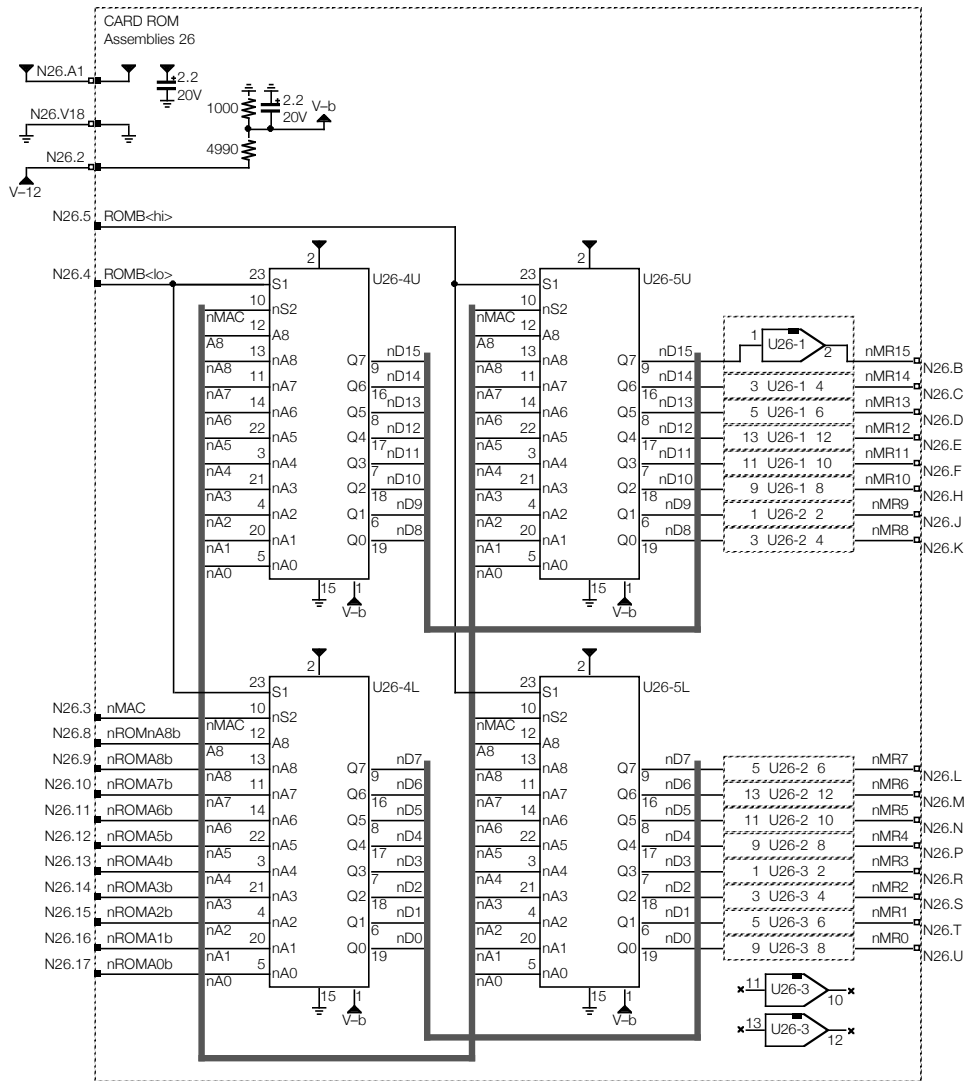
HP 9830 Computer

Section: ROM Addressing

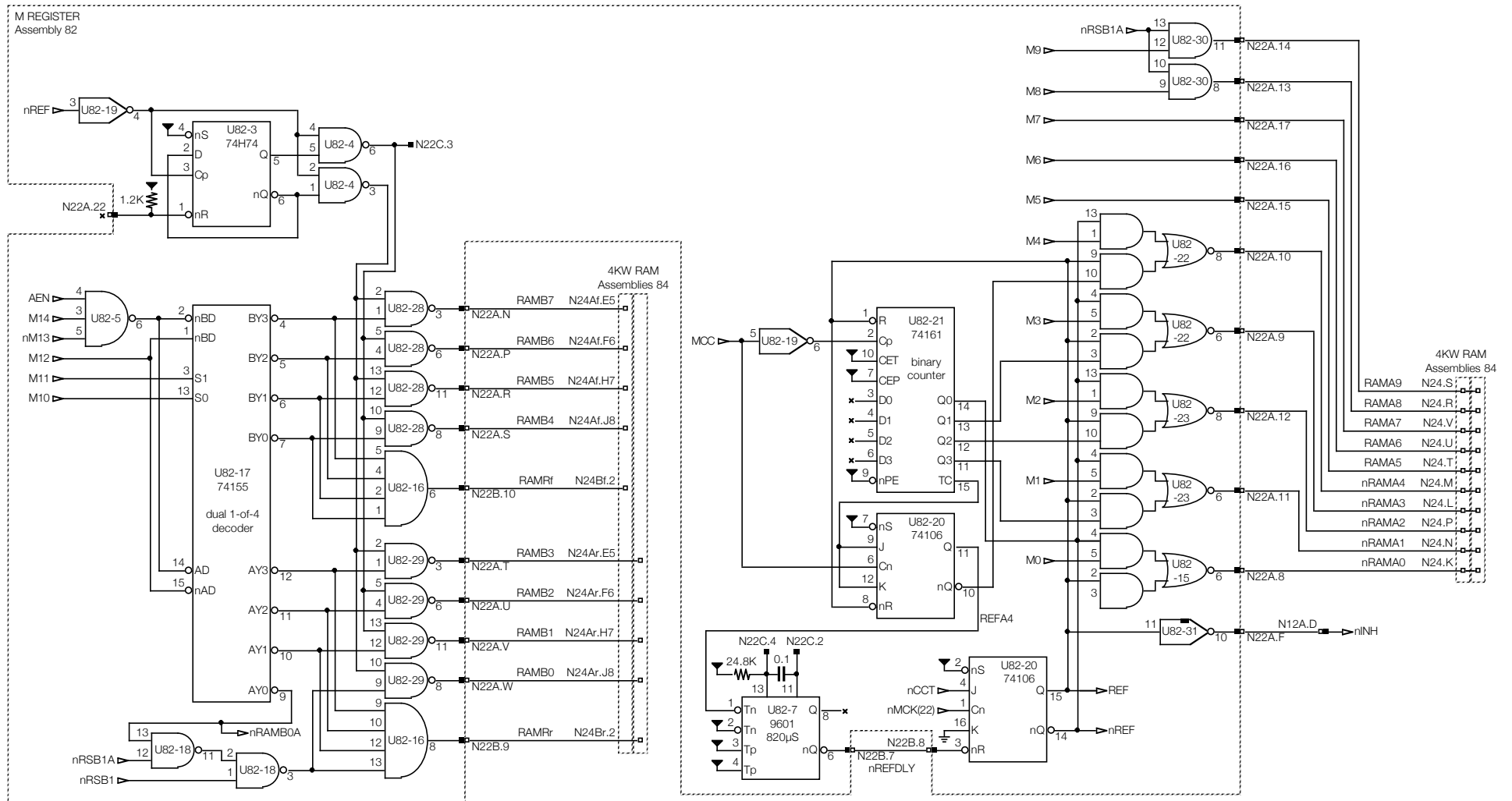
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Cartridge disassembly required for detail.
Presumably identical to Card ROM but without the data buffers.

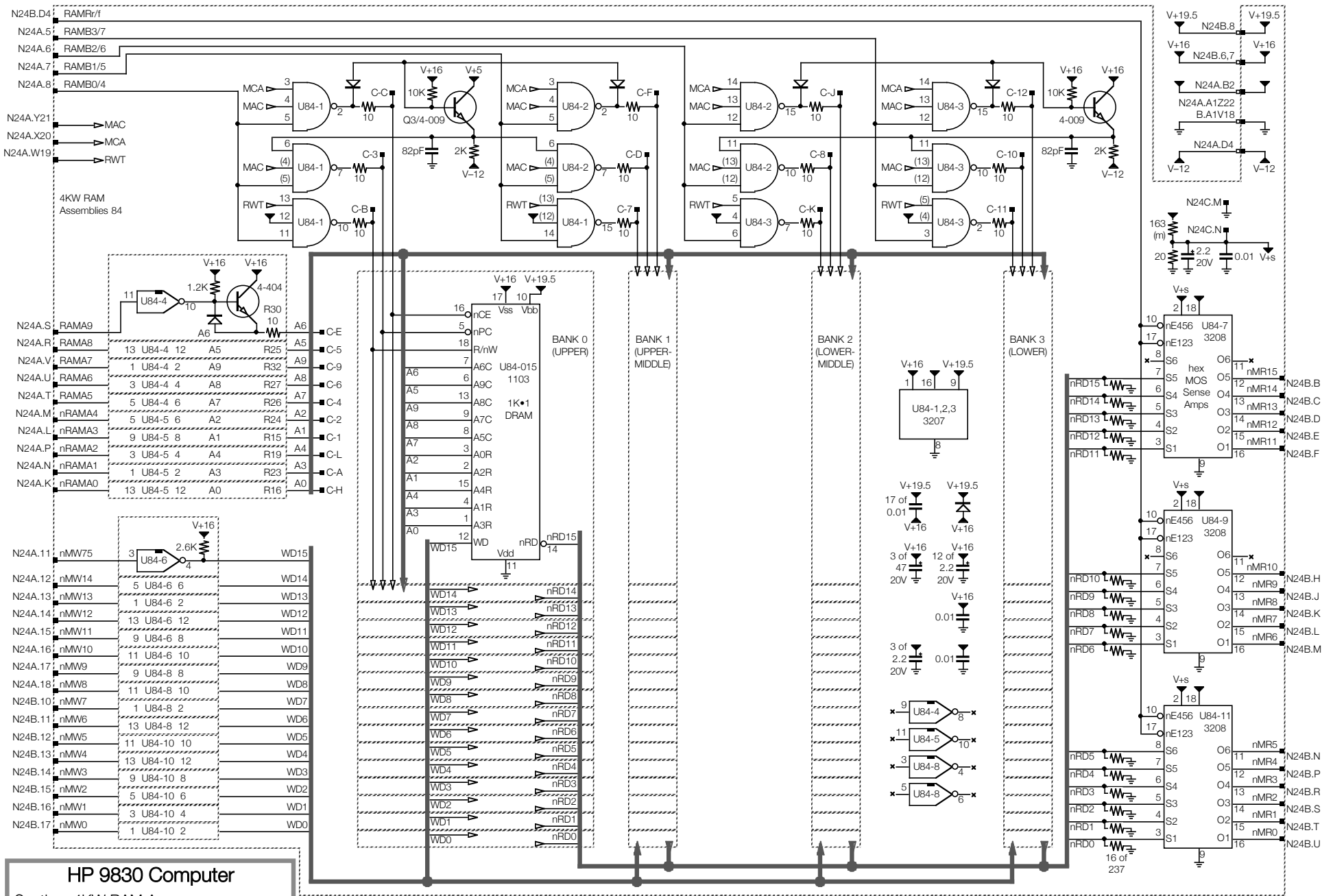


HP 9830 Computer

Section: RAM Addressing

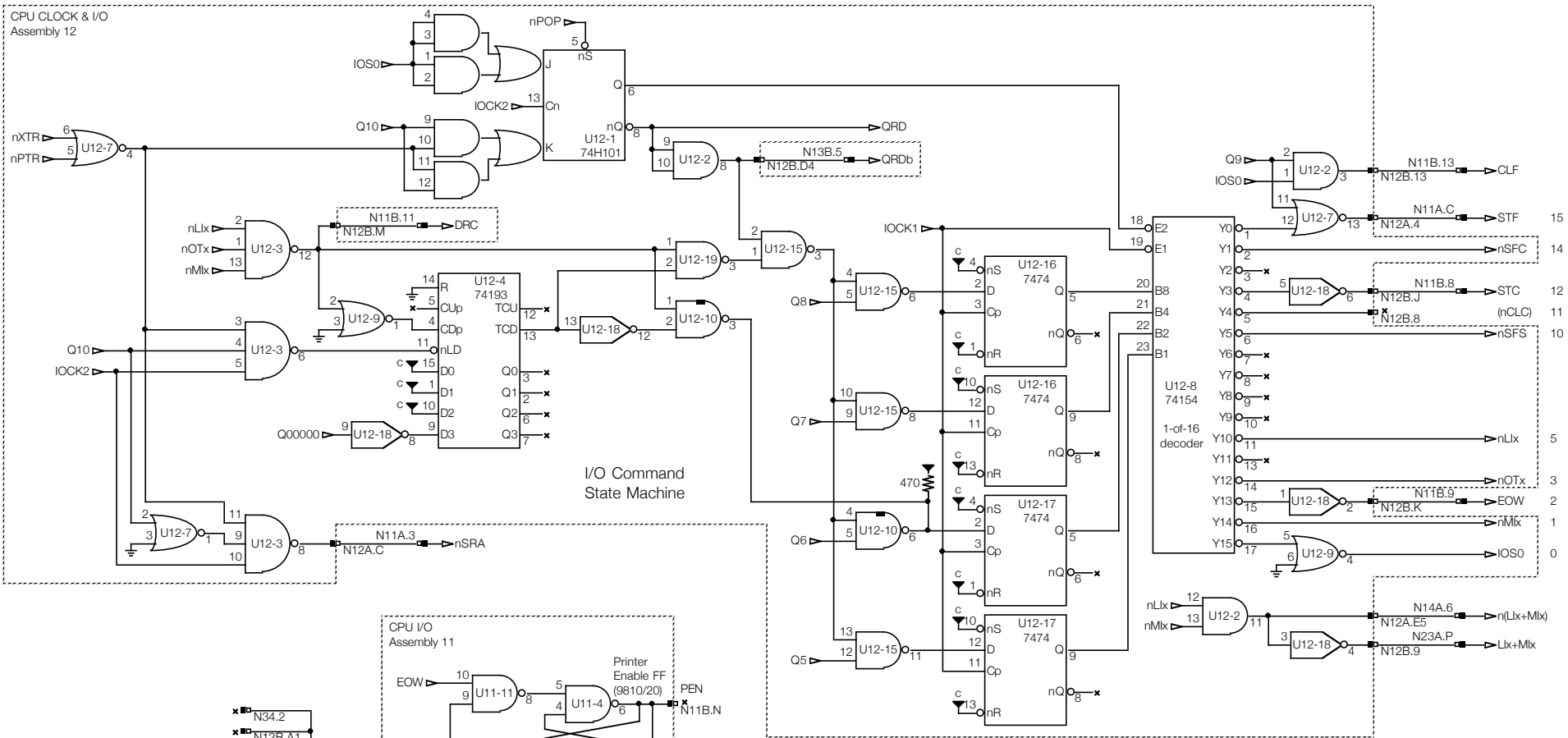
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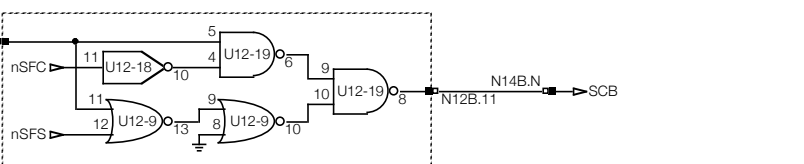
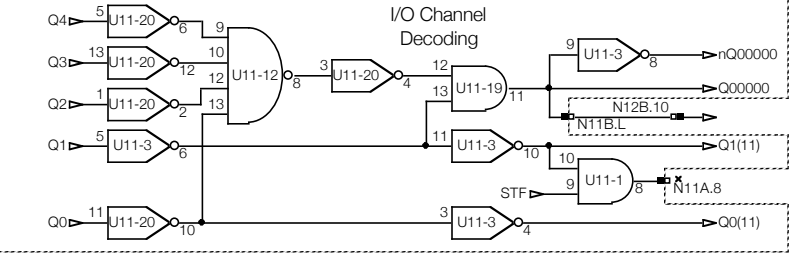
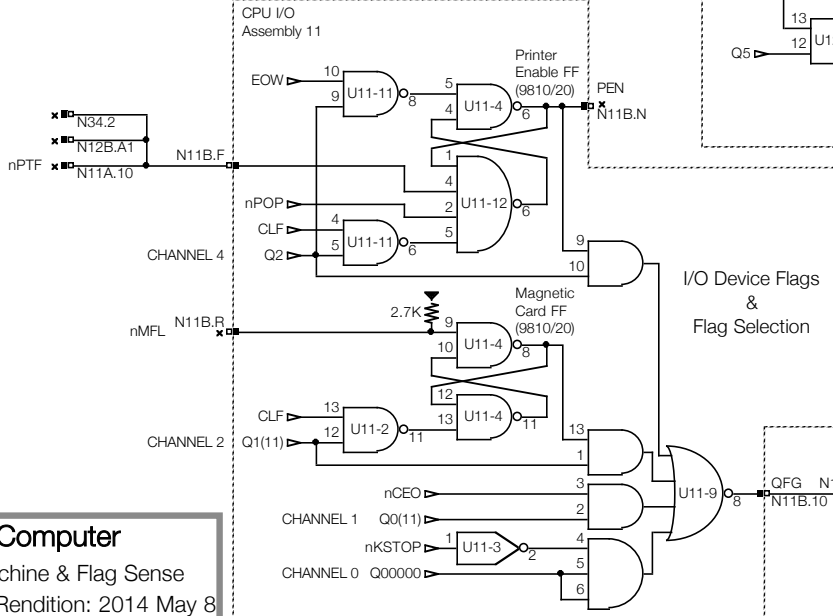


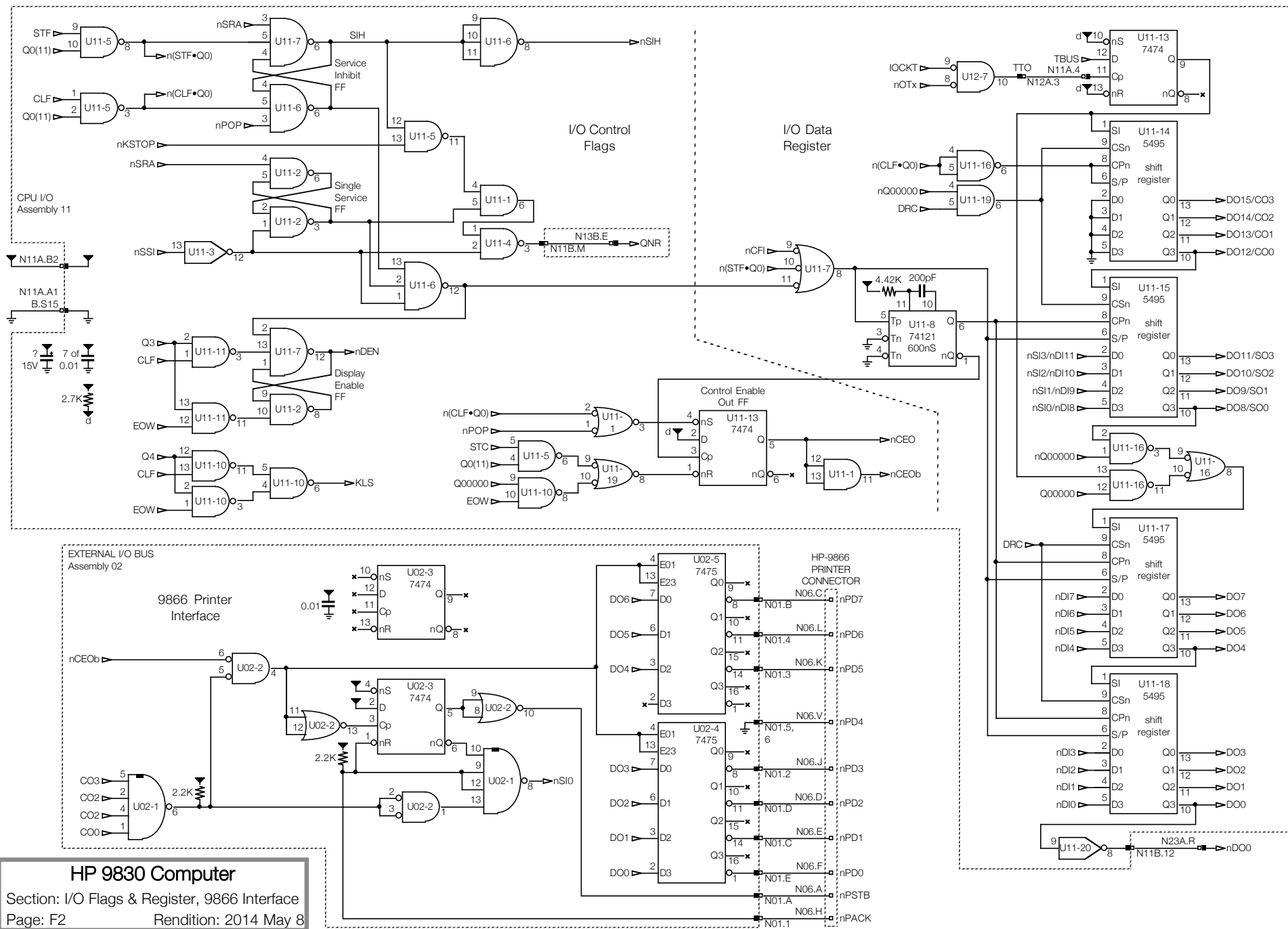
HP 9830 Computer
 Section: 4KW RAM Array
 Page: M8 Rendition: 2014 May 8

CPU CLOCK & I/O
Assembly 12



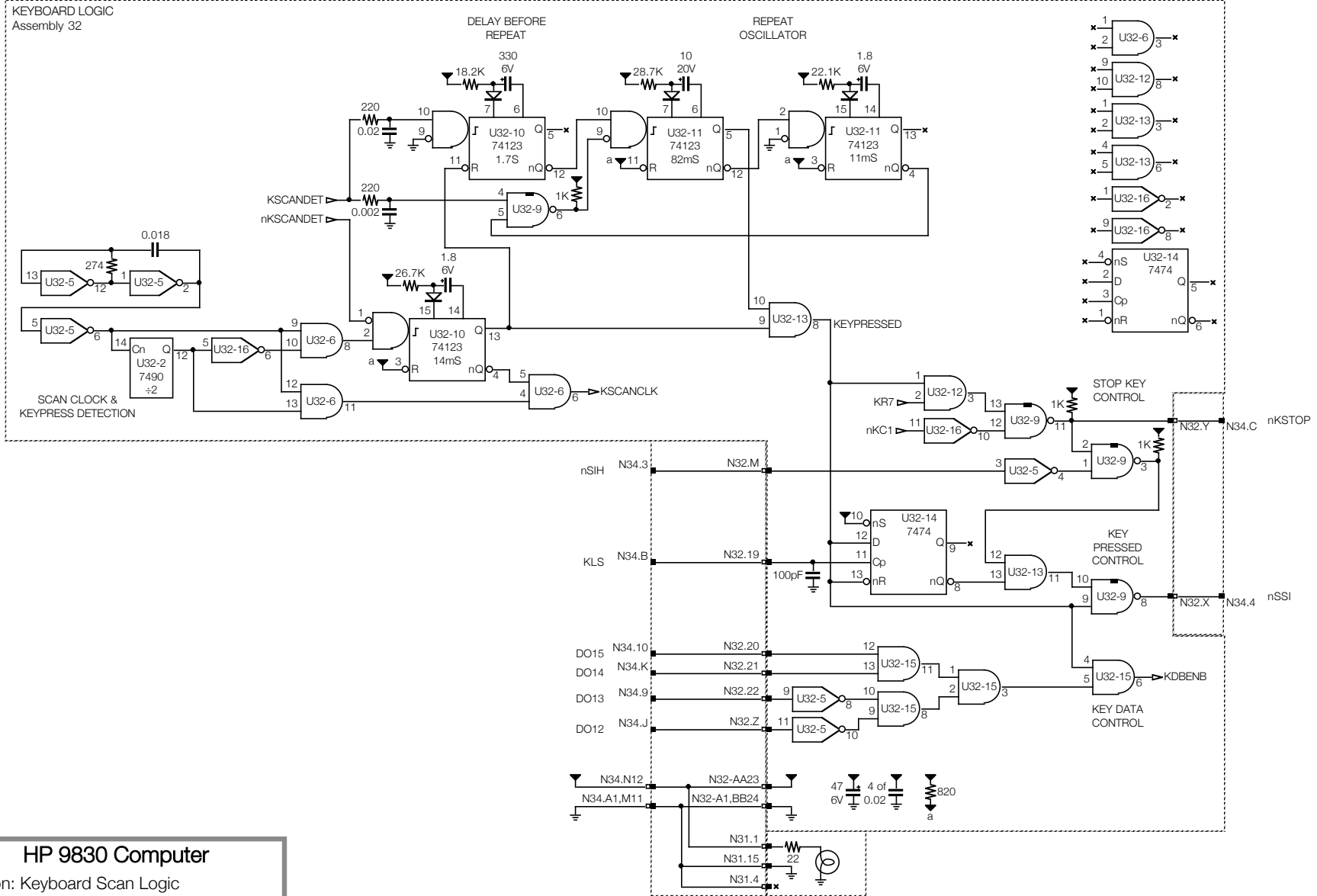
CPU I/O
Assembly 11





HP 9830 Computer
 Section: I/O Flags & Register, 9866 Interface
 Page: F2 Rendition: 2014 May 8

KEYBOARD LOGIC
Assembly 32

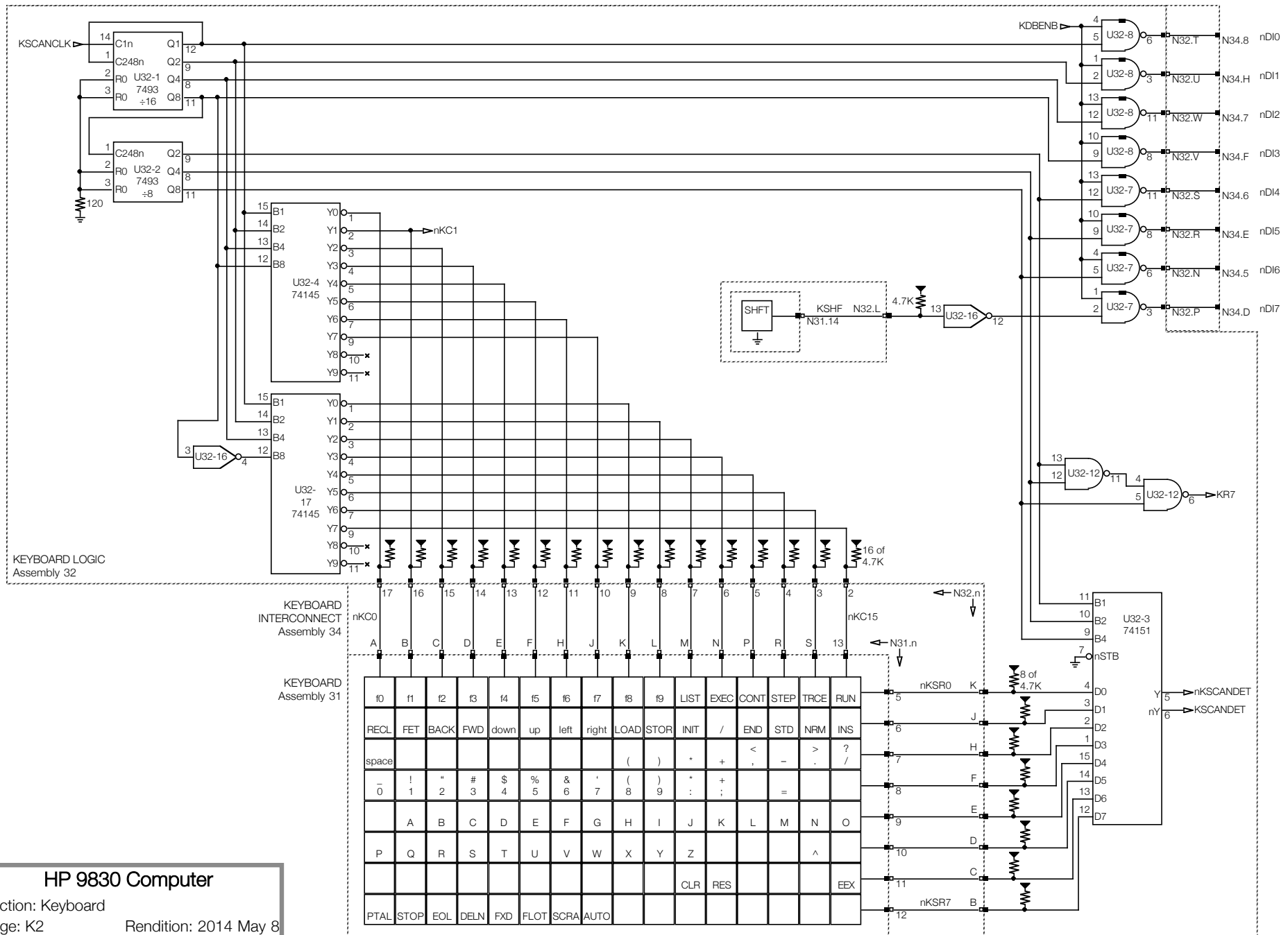


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Section: Keyboard Scan Logic

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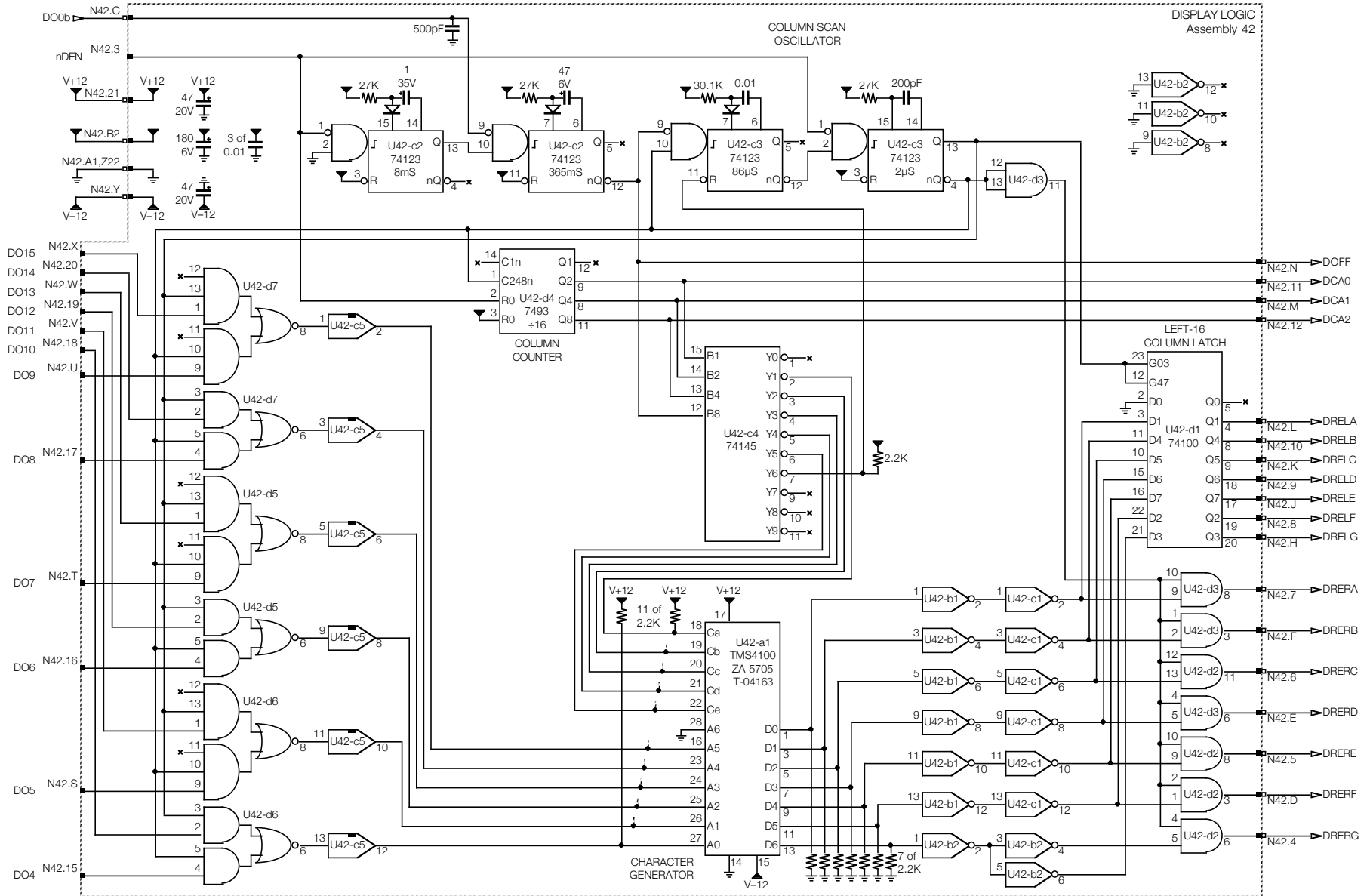


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Section: Keyboard

Page: K2

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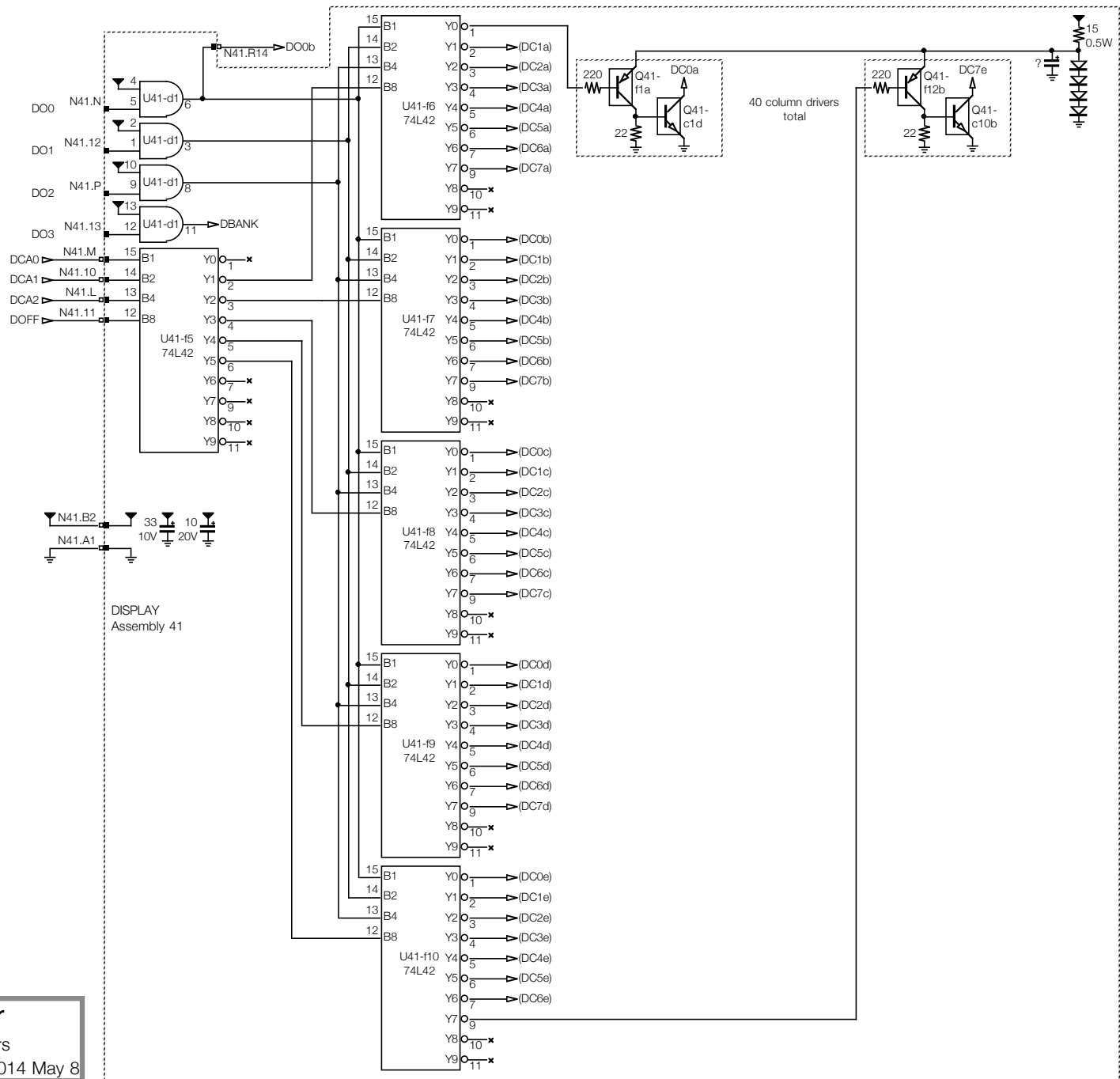


HP 9830 Computer

Section: Display Logic

Page: D1

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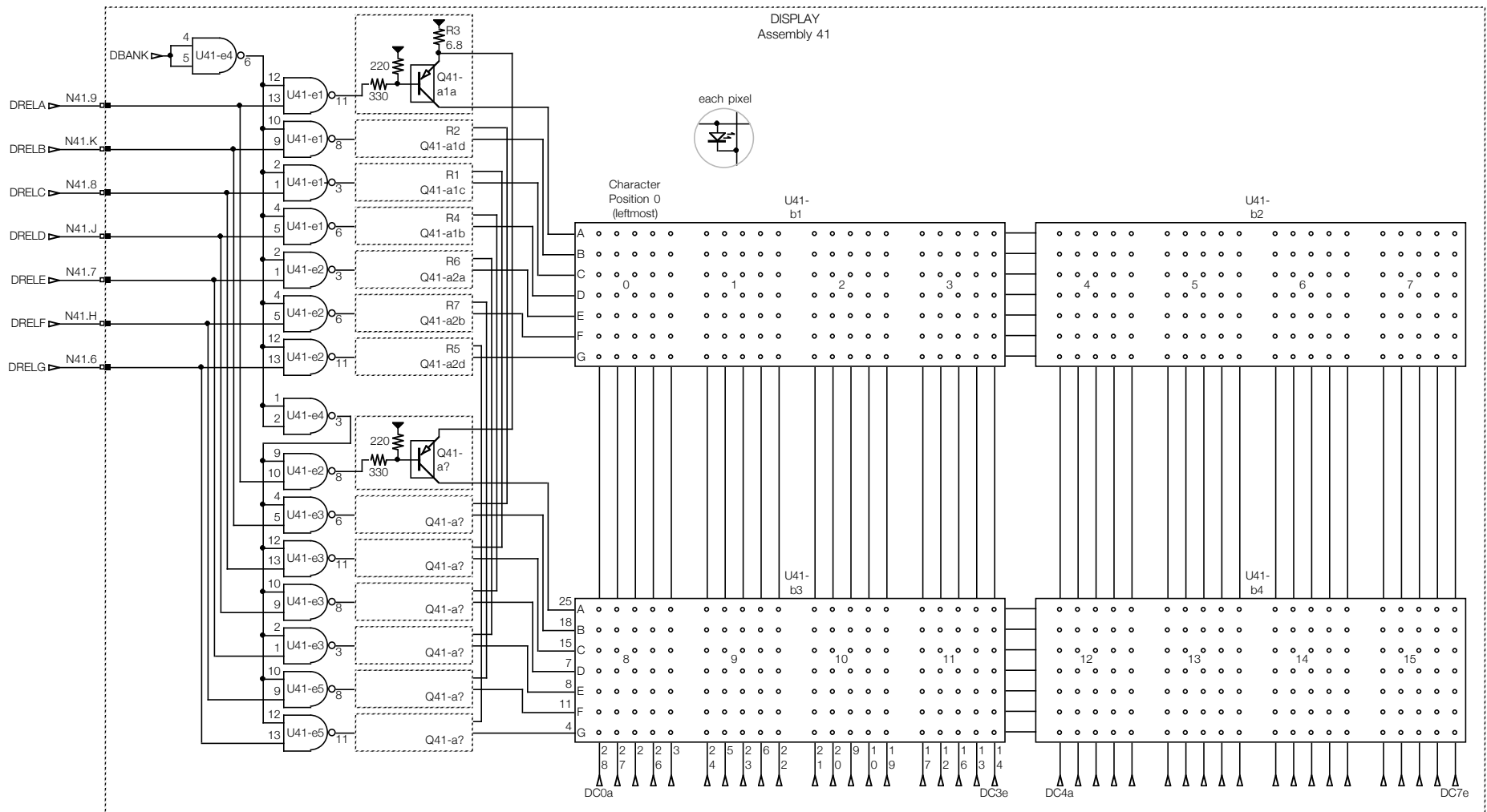


HP 9830 Computer

Section: Display Column Decoders

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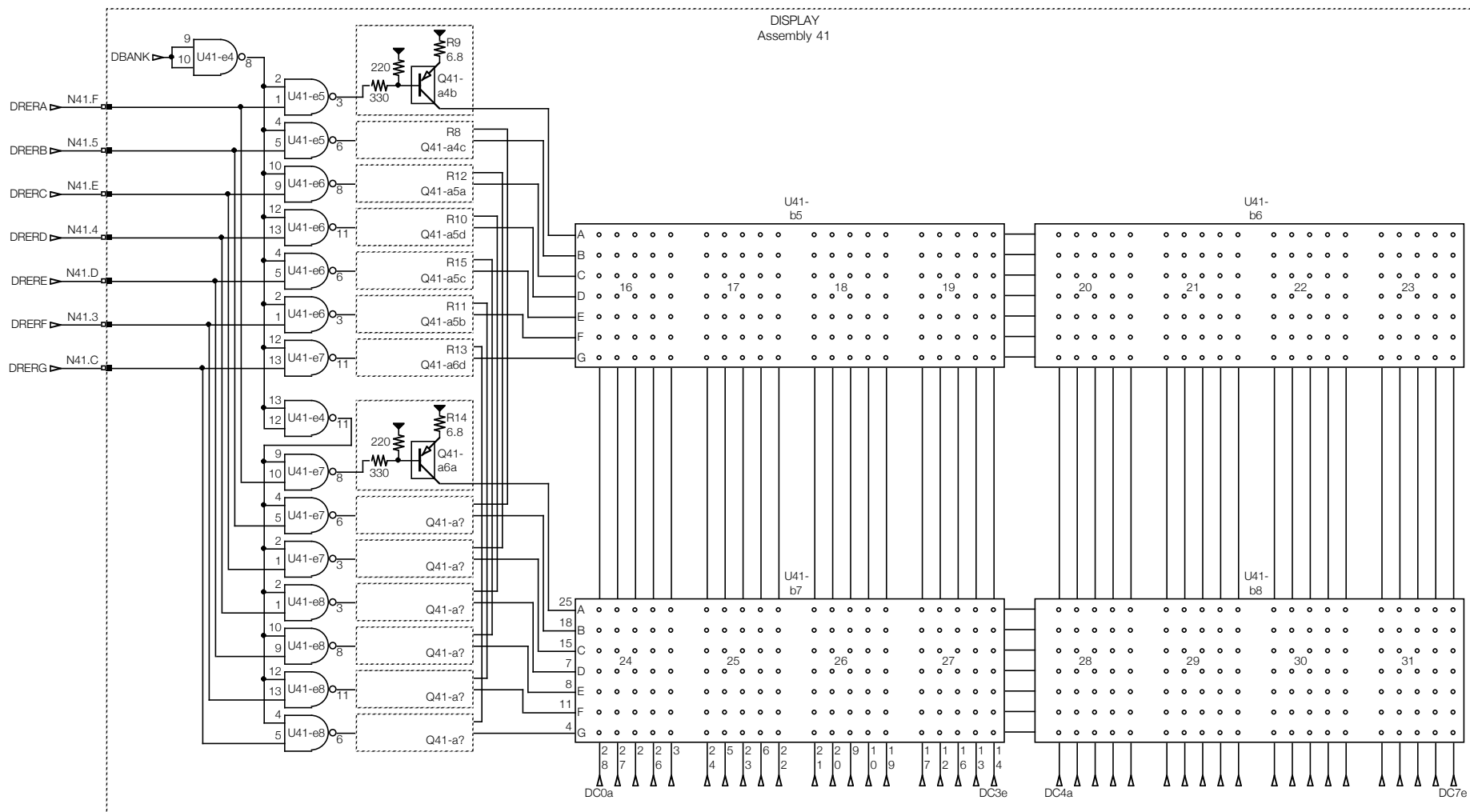
HP 9830 Computer

Section: Display Characters Left-16

Page: D3

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DISPLAY
Assembly 41

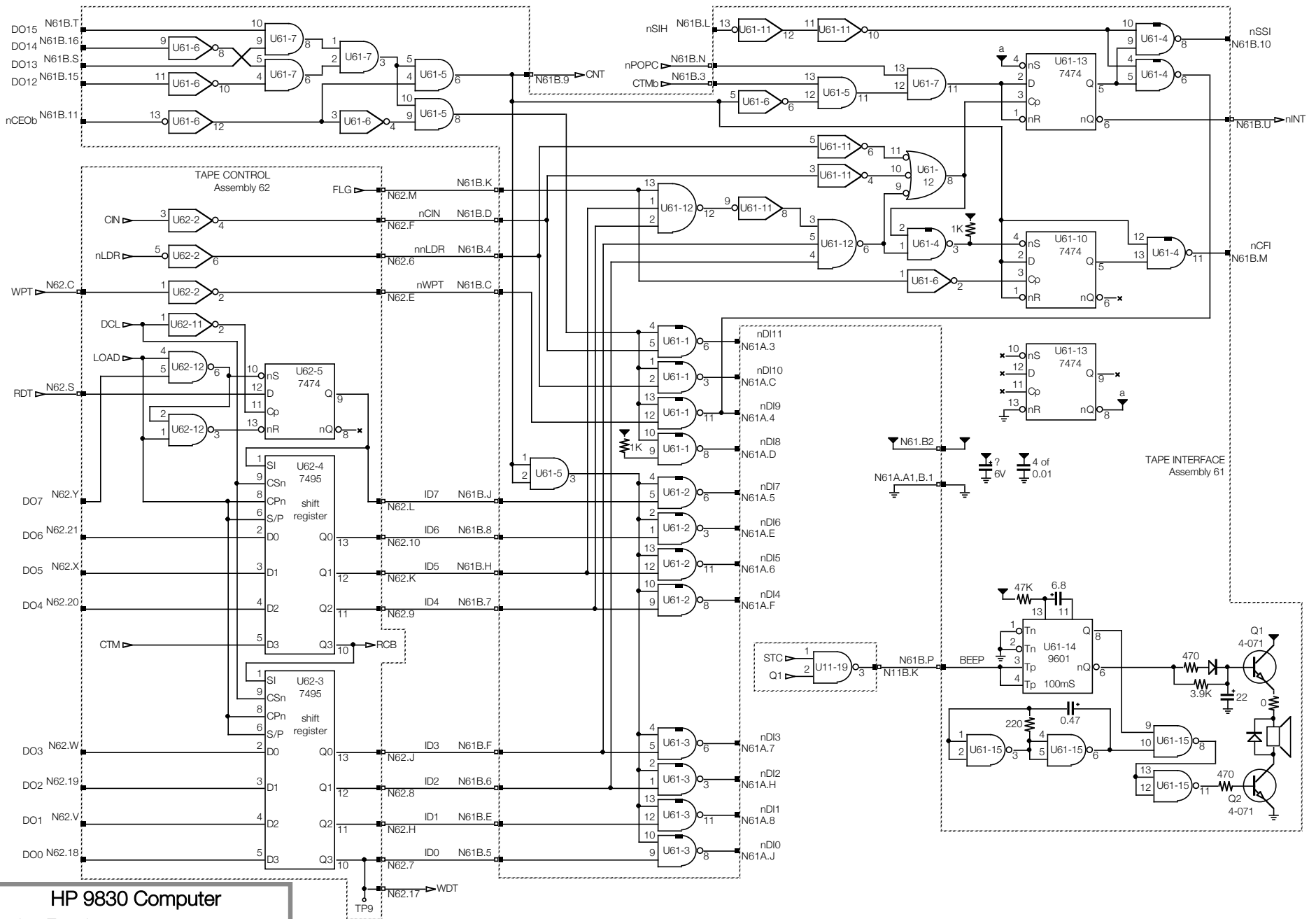


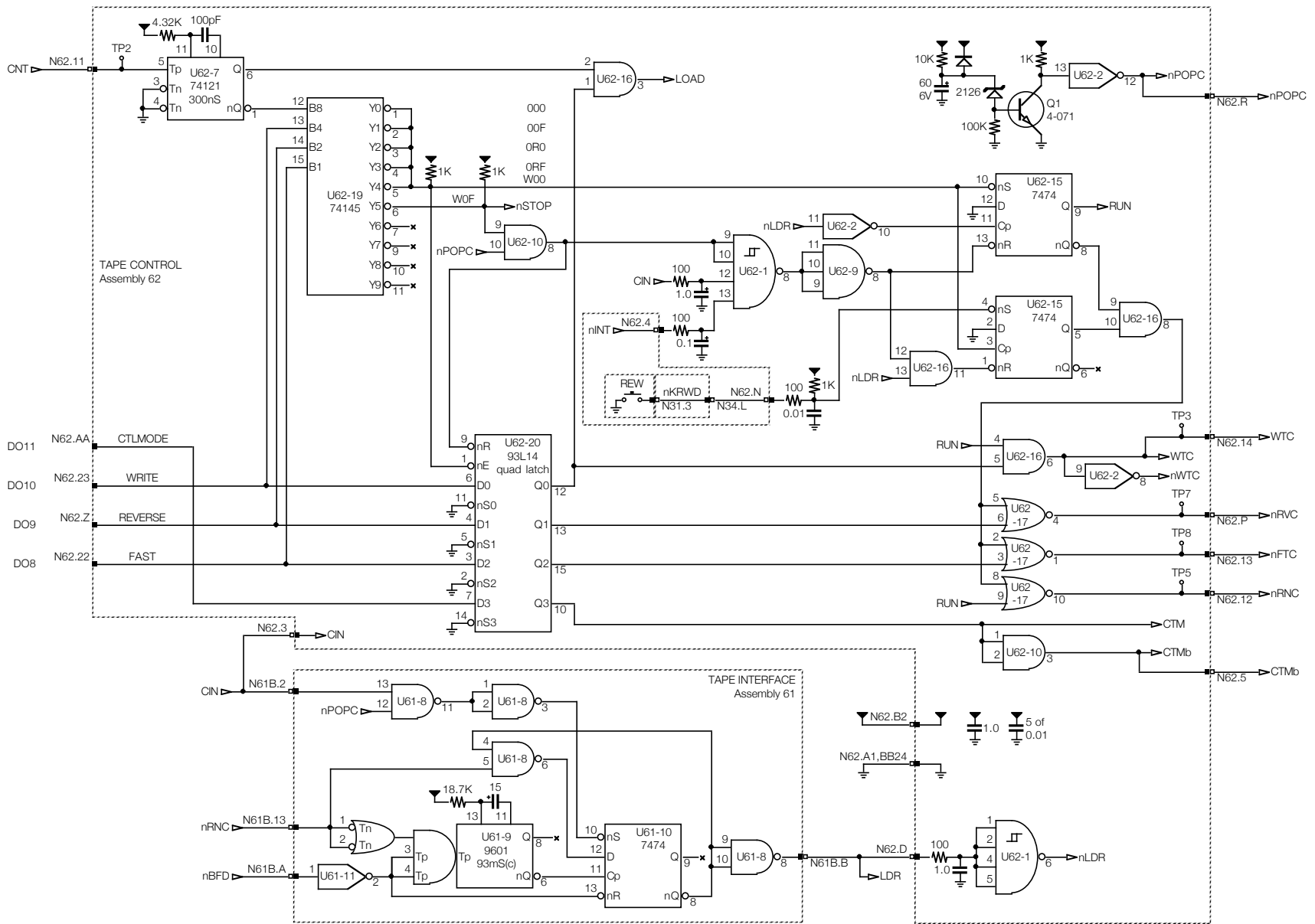
HP 9830 Computer

Section: Display Characters Right-16

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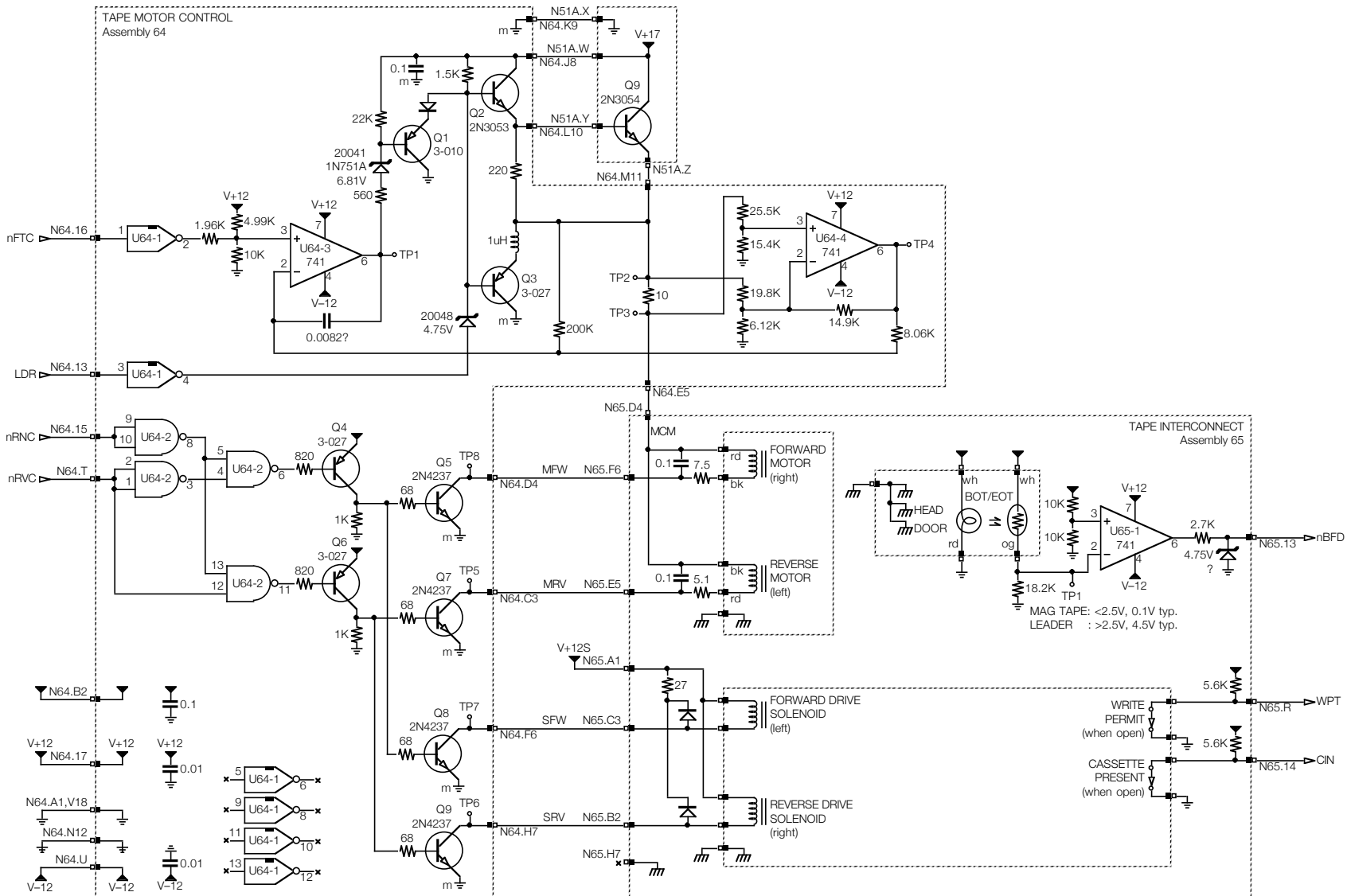


HP 9830 Computer

Section: Tape Command Decode

Page: T2

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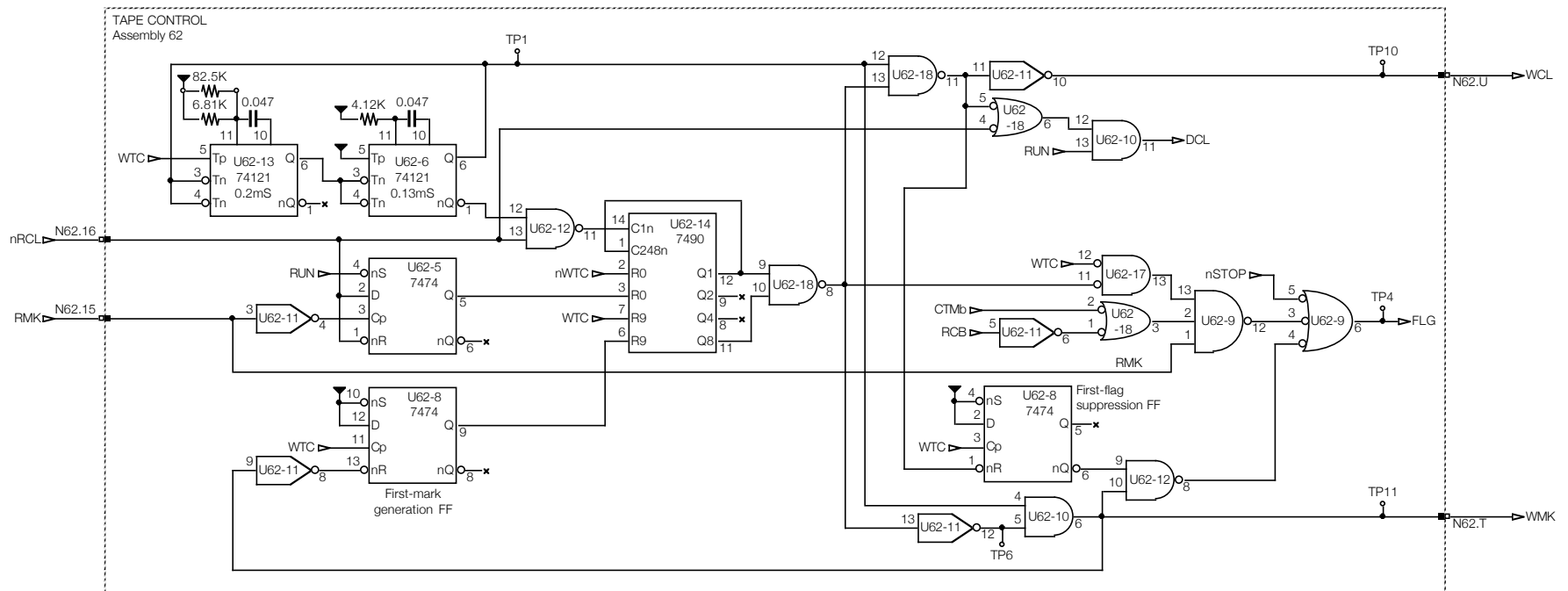


HP 9830 Computer

Section: Tape Drive

Page: T3

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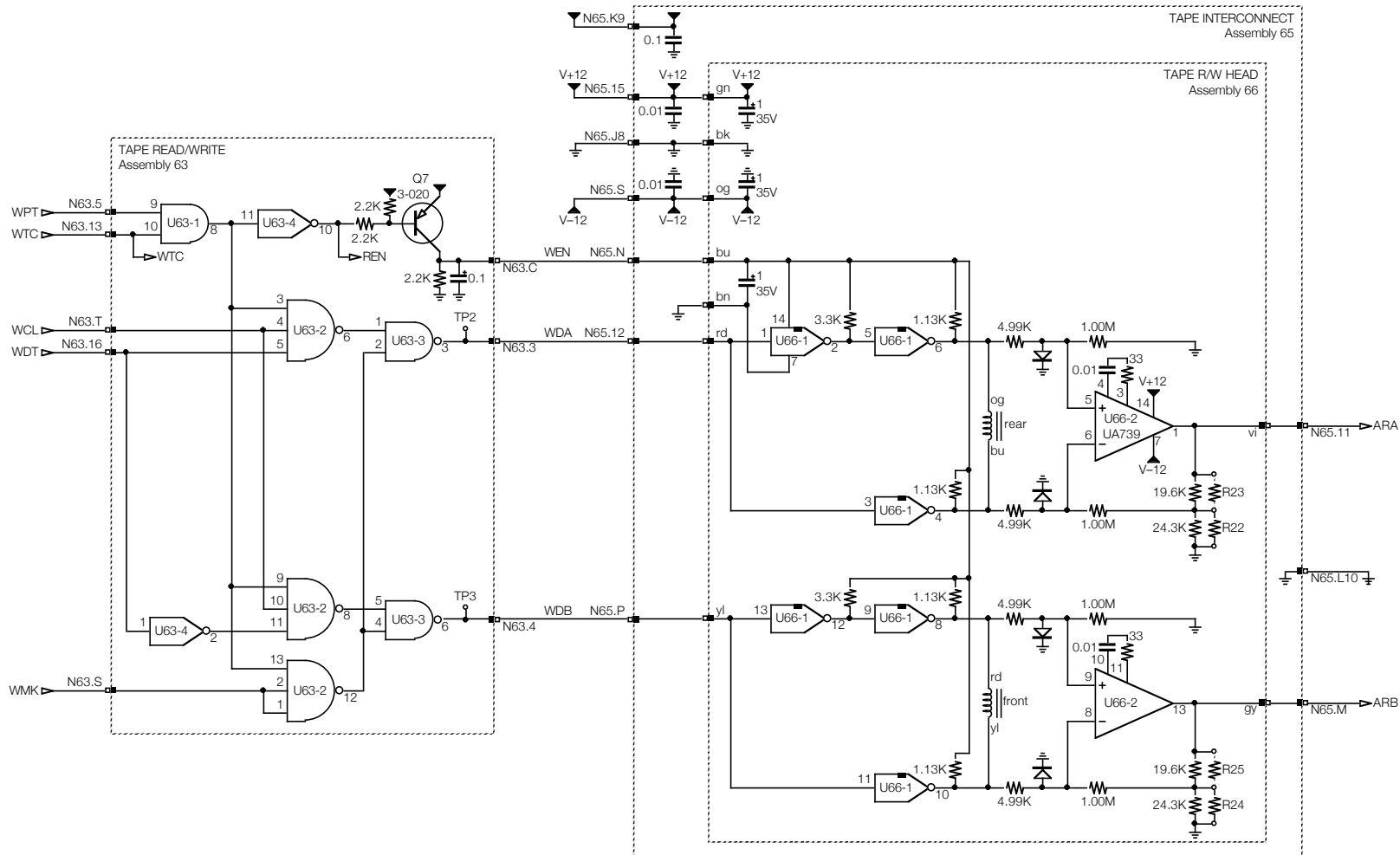


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Section: Tape Data Clock

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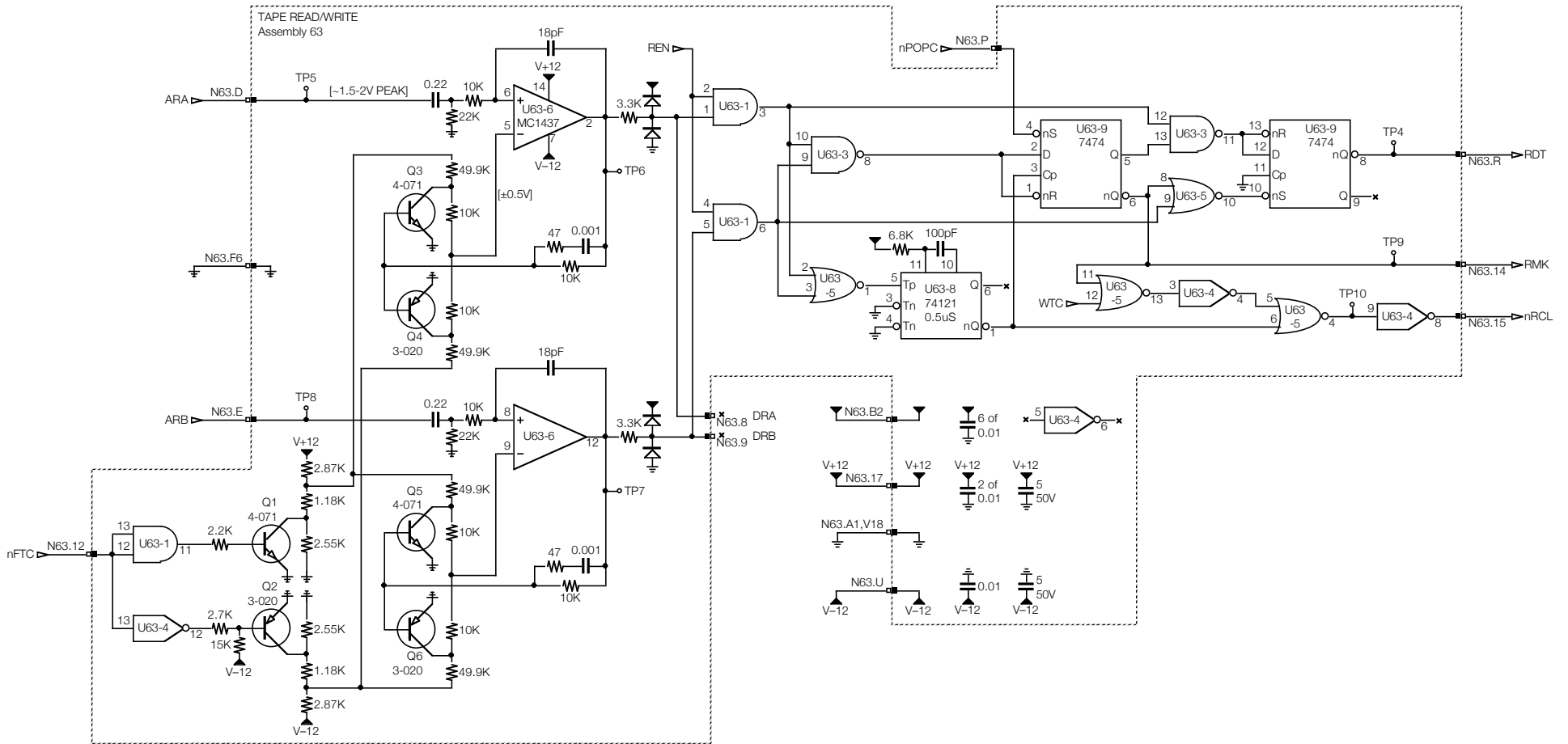
HP 9830 Computer

Section: Tape Read/Write

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	R22	R24
9830:	28.7K	28.7K
9865-0869:	24.3K	26.1K
9865-1570:	15.8K	15.8K

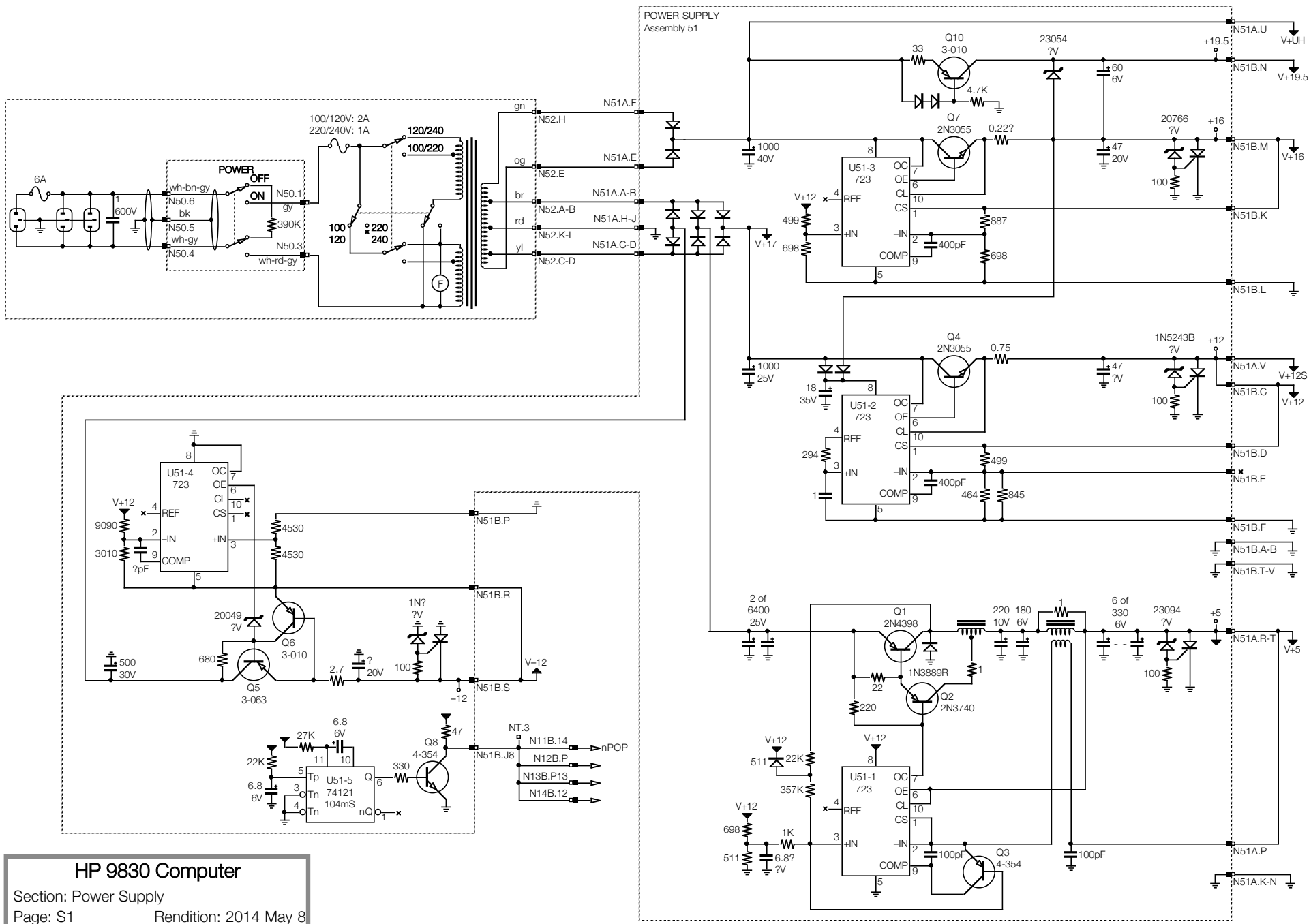


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Section: Tape Read

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 Section: Power Supply
 Page: S1 Rendition: 2014 May 8

IC Units

IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	IC	Type	
U02-1	74H22	U13-1	7404	U21-1	7416	U83-1	7402	U32-1	7493	U41-a1	(NPN)	U42-a1	TMS4100	U62-1	7413	BASIC I ROM		
	MC3012	U13-2	74H101	U21-2	7416	U83-2	74H52	U32-2	7493	U41-a2	(NPN)	U42-b1	74L04	U62-2	7404	U21-0L	1818-2064E	
U02-2	7402	U13-3	5495	U21-3	7416	U83-3	7495	U32-3	74151	U41-a3	(NPN)	U42-b2	74L04	U62-3	7495	U21-0U	1818-2065E	
U02-3	7474	U13-4	74H10	U21-4	7417	U83-4	7495	U32-4	74145	U41-a4	(NPN)	U42-c1	7404	U62-4	7495	U21-1L	1818-2066E	
U02-4	7475	U13-5	74150	U21-5	7417	U83-5	7495	U32-5	74S04	U41-a5	(NPN)	U42-c2	74123	U62-5	7474	U21-1U	1818-2067E	
U02-5	7475	U13-6	3601	U21-6	7417	U83-6	7495	U32-6	7408	U41-a6	(NPN)	U42-c3	74123	U62-6	74121	U21-2L	1818-2190A	
		U13-7	3601	U21-7	7417	U83-7	74H00	U32-7	7403	U41-a7	(NPN)	U42-c4	74145	U62-7	74121	U21-2U	1818-2191A	
U03-11	7417	U13-8	74H108	U21-8	7417	U83-8	74H54	U32-8	7403	U41-b1	(5*7 LED)	U42-c5	7407	U62-8	7474	U21-3L	1818-2070E	
U03-12	7417	U13-9	74H108	U21-9	7417	U83-9	74H08	U32-9	7403	U41-b2	(5*7 LED)	U42-d1	74100	U62-9	7410	U21-3U	1818-2071E	
U03-13	7417	U13-10	74155	U21-10	7417		MC3001	U32-10	74123	U41-b3	(5*7 LED)	U42-d2	7408	U62-10	7408	U21-4L	1818-2072E	
		U13-11	74H08	ROMS	(HP ROM)	U83-10	7404	U32-11	74123	U41-b4	(5*7 LED)	U42-d3	7408	U62-11	7404	U21-4U	1818-2073E	
U11-1	7408	U13-12	5495	U82-1	74106	U83-11	7404	U32-12	7408	U41-b5	(5*7 LED)	U42-d4	7493	U62-12	7400	U21-5L	1818-2074E	
U11-2	7400	U13-13	5495	U82-2	74H106	U83-12	7404	U32-13	7408	U41-b6	(5*7 LED)	U42-d5	7451	U62-13	74121	U21-5U	1818-2075E	
U11-3	7404	U13-14	5495	U82-3	74H74	U83-13	7404	U32-14	7474	U41-b7	(5*7 LED)	U42-d6	7451	U62-14	7490	U21-6L	1818-2194A	
U11-4	7400	U13-15	9322	U82-4	74H00	U83-14	7404	U32-15	7408	U41-b8	(5*7 LED)	U42-d7	7451	U62-15	7474	U21-6U	1818-2077E	
U11-5	7400	U13-16	74H108	U82-5	7410	U83-15	7404	U32-16	7404	U41-c1	(PNP)			U62-16	7408	U21-7L	1818-2078E	
U11-6	7410	U13-17	74H108	U82-6	7432	U84-1	3207	U32-17	74145	U41-c2	(PNP)	U51-1	723	U62-17	7402	U21-7U	1818-2079E	
U11-7	7410	U13-18	74155	U82-7	9601	U84-2	3207			U41-c3	(PNP)	U51-2	723	U62-18	7400	U21-10L	1818-2080E	
U11-8	74121	U13-19	3301A	U82-8	7495	U84-3	3207			U41-c4	(PNP)	U51-3	723	U62-19	74145	U21-10U	1818-2081E	
U11-9	7453	U13-20	3301A	U82-9	7495	U84-4	7406			U41-c5	(PNP)	U51-4	723	U62-20	93L14	U21-11L	1818-2082E	
U11-10	7400	U13-21	3301A	U82-10	7495	U84-5	7406			U41-c6	(PNP)	U51-5	74121			U21-11U	1818-2083E	
U11-11	7400	U13-22	3301A	U82-11	7495	U84-6	7406			U41-c7	(PNP)			U63-1	7408	U21-12L	1818-2084E	
U11-12	7420	U13-23	3601	U82-12	7408	U84-7	3208			U41-c8	(PNP)	U61-1	7403	U63-2	7410	U21-12U	1818-2085E	
U11-13	7474			U82-13	7400	U84-8	7406			U41-c9	(PNP)	U61-2	7403	U63-3	7400	U21-13L	1818-2086E	
U11-14	5495	U14-1	5495	U82-14	74H11	U84-9	3208			U41-c10	(PNP)	U61-3	7403	U63-4	7404	U21-13U	1818-2087E	
U11-15	5495	U14-2	74H62	U82-15	74H51	U84-10	7406			U41-d1	7408	U61-4	7403	U63-5	7402	U21-14L	1818-2182A	
U11-16	7400	U14-3	74H53	U82-16	74H21	U84-11	3208			U41-e1	7400	U61-5	7408	U63-6	MC1437	U21-14U	1818-2183A	
U11-17	5495	U14-4	5495	U82-17	74155	RAMS	1103			U41-e2	7400	U61-6	7404	U63-8	74121	U21-15L	1818-2184A	
U11-18	5495	U14-5	5495	U82-18	7400					U41-e3	7400	U61-7	7408	U63-9	7474	U21-15U	1818-2185A	
U11-19	7408	U14-6	7491	U82-19	7404	U25-1	7417			U41-e4	7400	U61-8	7400					
U11-20	7404	U14-7	74H00	U82-20	74H106	U25-2	7417			U41-e5	7400	U61-9	9601	U64-1	7406	BASIC II Card ROM		
		U14-8	74H08	U82-21	74161	U25-3	7416			U41-e6	7400	U61-10	7474	U64-2	MC846	09830-66526		
U12-1	74H10	U14-9	9328	U82-22	74H51	U25-4	7416			U41-e7	7400	U61-11	7404	U64-3	741	U26-4L	1818-?	
U12-2	7408	U14-10	9328	U82-23	74H51	U25-5	7416			U41-e8	7400	U61-12	7410	U64-4	741	U26-4U	1818-?	
U12-3	7410	U14-11	3601	U82-24	7437	U25-6	74154			U41-e9	(NPN)	U61-13	7474			U26-5L	-	
U12-4	74193	U14-12	7474	U82-25	7400					U41-e10	(NPN)	U61-14	9601	U65-1	741	U26-5U	-	
U12-5	74H00	U14-13	74H00	U82-26	74H04	U26-1	7417			U41-e11	(NPN)	U61-15	7400					
U12-6	74H74	U14-14	74H21	U82-27	7408	U26-2	7417			U41-e12	(NPN)			U66-1	7406	String Variables Card ROM		
U12-7	7402	U14-15	7432	U82-28	7400	U26-3	7417			U41-f1	(NPN)	U66-2	UA739			11271-66520		
U12-8	74154	U14-16	N8885A	U82-29	7400	ROMS	(HP ROM)			U41-f2	(NPN)			U26-4L	1818-2186A	B-636D		
U12-9	7402	U14-17	74H00	U82-30	7408					U41-f3	(NPN)			U26-4U	1818-2187A	B-675B		
U12-10	7403	U14-18	74H00	U82-31	7416					U41-f4	(NPN)			U26-5L	1818-2188A	B-656B		
U12-11	74H00	U14-19	3601	U82-32	74154					U41-f5	74L42			U26-5U	1818-2189A	B-741C		
U12-12	74H20	U14-20	74H01	U82-33	7400					U41-f6	74L42					Plotter Card ROM		
U12-13	74H40			U82-34	7400					U41-f7	74L42					11271-66520		
U12-14	74193									U41-f8	74L42					U26-4L	1818-2116B	B-805B
U12-15	7400									U41-f9	74L42					U26-4U	1818-2117B	C-033D
U12-16	7474									U41-f10	74L42					U26-5L	1818-2118B	C-071A
U12-17	7474									U41-f11	(NPN)					U26-5U	1818-2119B	C-083A
U12-18	7404									U41-f12	(NPN)							
U12-19	7400																	

Count: 306
Req. ROMS: 30

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Section: IC Units List

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IC Types & Power Pins

Type	HP #	V+5 GND Function	Qty.	Type	HP #	V+5 GND Function	Qty.
7400	1820-0054	14 7 NAND 2-in / quad	28	74100	24 7 4-bit latch / dual		1
74H00	1820-0370	14 7 "	8	74H101	14 7 FF JK		1
74H01	1820-0605	14 7 NAND 2-in OC / quad	1	74106	5 13 FF JK / dual		1
7402	1820-0328	14 7 NOR 2-in / quad	6	74H106	5 13 "		2
7403	1820-0269	14 7 NAND 2-in OC / quad	8	74H108	14 7 FF JK /dual		4
7404	1820-0174	14 7 NOT / hex	18	74121	14 7 monostable		6
74H04	1820-0424	14 7 "	1	74123	16 8 monostable /dual		4
74L04	14 7 "	2	74145	16 8 decoder 1-of-10 OC		4	
74S04	14 7 "	1	74150	24 12 multiplexer 16-in		1	
7406	1820-0471	14 7 NOT OC hi-V / hex	7	74151	16 8 multiplexer 8-in		1
7407	14 7 buffer OC hi-V / hex	1	74154	1820-0495 24 12 decoder 1-of-16		3	
7408	1820-0511	14 7 AND 2-in / quad	18	74155	16 8 decoder 1-of-4 / dual		3
74H08	14 7 "	2	74161	16 8 counter 4-bit binary syncl		1	
74H08/M	1820-0141	14 7 "	1	74193	1820-0233 16 8 counter 4-bit binary up/di		2
7410	1820-0068	14 7 NAND 3-in/ triple	7	93L14	1820-0701 16 8 latch 4-bit		1
74H10	1820-0371	14 7 "	2	9322	1820-0616 16 8 multiplexer 2-in / quad		1
74H11	14 7 AND 3-in/ triple	1	9328	1820-0741 16 8 SR 8-bit /dual		2	
7413	1820-0537	14 7 NAND 4-in schmitt /dual	1	9601	1820-0207 14 7 monostable		3
7416	1820-0577	14 7 NOT OC hi-V buffer / hex	7				
7417	1820-0618	14 7 buffer OC hi-V / hex	15	MC846	1820-0094 14 7 NAND 2-in DTL / quad		1
7420	14 7 NAND 4-in /dual	1	N8885A	1820-0923 14 7 NOR 2-in / quad		1	
74H20	14 7 "	1					
74H21	1820-0374	14 7 AND 4-in / dual	2	1103	* RAM 1K*1		128
74H22	14 7 NAND 4-in OC /dual	1	3207	* drivers for 1103s / quad		3	
7432	1820-0661	14 7 OR 2-in / quad	2	3208	* amps for 1103s / hex		3
7437	14 7 NAND 2-in buffer / quad	1	3301A	16 8 ROM 256*4		4	
74H40	1820-0376	14 7 NAND 4-in buffer / dual	1	3601	16 8 ROM 256*4		5
74L42	1820-0777	16 8 decoder 1-of-10	6	(HP ROM)	* ROM 512*8		30
7451	14 7 AOI 2-2 / dual	3	TMS4100	* ROM char. gen.		1	
74H51	1820-0378	14 7 "	3	(5*7 LED) 1990-0343	- 5*7 LED display / quad		8
74H52	14 7 AO 2-2-2-3-e	1	723	1820-0196 * voltage regulator		4	
7453	14 7 AOI 2-2-2-2-e	1	UA739	1826-0044 * linear amp / dual		1	
74H53	1820-0380	14 7 AOI 2-2-2-3-e	1	741	1820-0203 * op amp		3
74H54	14 7 AOI 2-2-2-2	1	MC1437L	1826-0019 * op amp / dual		1	
74H62	1820-0385	14 7 AO expander 2-2-3-3	1	(NPN) 1858-0014	- transistors NPN / quad		17
7474	1820-0077	14 7 FF D / dual	12	(PNP) 1858-0027	- transistors PNP / quad		10
74H74	1820-0512	14 7 "	2				
7475	1820-0301	5 12 latch 4-bit	2				
7490	5 10 counter decade	1					
7491	1820-0364	5 10 SR 8-bit	1				
7493	5 10 counter 12	3					
7495	1820-0367	14 7 SR 4-bit	10				
5495	14 7 "	11					

43

203

34

261

Number of IC types: 77
 Number of ICs: 464
 Check: 464

* See circuit schematic for power connections

Monostable Pulse Time Calculations

IC	Type	C uF	R KOhm	t uS	t mS
U11-b4	74121	0.0002	4.42	0.613	
U82-7	9601	0.1	24.8	816	
U32-10	74123	330	18.2		1,746
U32-10		1.8	26.7		14
U32-11	74123	10	28.7		82
U32-11		1.8	22.1		11
U42-c2	74123	47	27		365
U42-c2		1	27		8
U42-c3	74123	0.01	30.1	86	
U42-c3	123 graph	0.0002	27	2	
U51-5	74121	6.8	22		104
U61-9	9601	15	18.7		93
U61-14	9601	6.8	47		104
U62-7	74121	0.0001	4.32	0.299	
U62-6	74121	0.047	4.12	134	
U62-13	74121	0.047	6	205	
U63-8	74121	0.0001	6.8	0.471	

Tape Head Amp Calculations

Divider U	19.6
Divider L	24.3
Divider L	16.8
Feedback R	1000
Series R	4.99
divider ratio	2.97
gain ratio	201.40
Gain	599
Output V (meas.)	1.5
Head V	0.0025

IC Notes

- 3301A microcode and 3601 ALU ROMS are pin-compatible with 74S387
 74S387: TI Memory Databook 1st Ed., 1975, pg 182.

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Section: IC Types List, Calculations

Page: A2

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CPU Clock

MCK	Master Clock \ 8MHz \ HPP: Memory Clock
SCK	Shift Clock \ basic bit-serial clock
RCK	ROM Clock \ defines one microcode cycle
nCCT	
nINH	Inhibit Clock \ OC line, normally used by memory system to stop processor during refresh. Single stepping control according to patent.
nIHC	Inhibit Clock \ turns off internal clock
XTC	External Clock
IOCK1	I/O Clock 1 \ for state machine
IOCK2	I/O Clock 2 \ for state machine
IOCKT	I/O Clock for transfer from T-bus

CPU Data

RBUS	ALU input
SBUS	ALU input
TBUS	ALU output
A<0..3>	A register outputs
B0	B register LSB
E0	E register LSB
P0	P register LSB (program counter)
Q<0..11>	Q register outputs (instruction register)
T<0..3>	T register outputs
BC	Binary Carry flag
DC	Decimal Carry flag

CPU Controls

POP	Power-On Pulse
MCDIS	Microcode DISable
nCCO	Control of shift Clock
nIPS	
CEM	
AC<0..2>	ALU function select
UTR	Unary to R-bus
PTR	P-reg to R-bus
QTR	Q-reg to R-bus
BCD	BCD ALU operation
XTR	A/B-reg to R-bus
MTS	M-reg to S-bus
TTS	T-reg to S-bus
SC0	S-bus Selector bit 0
SC1	S-bus Selector bit 1

Memory

RDM	Read Memory
WTM	Write Memory
AEN	Address ENable
MEN	Memory ENable
REF	Refresh RAM
RWT	Read/WriTe to RAM
REFDLY	Refresh Delay
MCP	Memory Cycle state-machine flag
MCA	Memory Cycle state-machine flag
MCB	Memory Cycle state-machine flag
MCC	Memory Cycle state-machine flag
MAC	Memory ACcess
MTS	M register to S-bus
TTM	T-bus to M register
M<0..15>	M Register (Memory Address)
MR<0..15>	Memory Read bus
MRC<0..15>	Memory Read bus for Cartridges
MW<0..15>	Memory Write bus
ROMB<00..37>	ROM Bank select
ROMA<0..8>	ROM Address
ROMA<0..8>b	ROM Address buffered
RSB1	another version of ROM Bank Select
RAMA<0..9>	RAM Address Bits
RAMB<0..7>	RAM Bank select
RAMR<a,b>	RAM boARd select
T<0..3>	T register outputs
TRI	T Register serial Input
TSC	T register Serial Clock
TPC	T register Parallel load Clock
TMC	T register Mode Control \ serial/parallel
EMB	Extended Memory Busy
MSTL	Memory Suppress T-register Load
EDT	External memory Data Transfer
XIN	External serial data IN

I/O

CO<0..3>	Device Select-Code Output Bus
SO<0..3>	State/Command Output Bus
DO<0..15>	Data Output Bus
SI<0..3>	Status Input Bus
DI<0..15>	Data Input Bus
CEO	Control Enable Output \ initiate I/O, enable device
SIH	Service Inhibit \ suppress interrupt
SSI	Service Request Strobe Input \ interrupt request
CFI	Channel Flag In \ ack/ready from device
SRA	Service Request Acknowledge \ interrupt ack
QNR	Not service r equest \ interrupt request
QRD	Qualifier ROM Disable \ disable proc during IO
QFG	Qualifier Flag \ for skip-flag instructions
SCB	Set Carry Bit
Q00000	5 LSBits of Q = 0 \ I/O channel 0
DRC	Data (IO) Register Clock
TTO	T-bus To Output (IOR)
CLC	Clear Control bit IO state
STC	Set Control bit IO state
CLF	Clear Flag IO state
STF	Set Flag IO state
SFC	Skip if Flag Clear IO state
SFS	Skip if Flag Set IO state
OTx	Output A/B IO state
Llx	Load Into A/B IO state
Mlx	Merge Into A/B IO state
EOW	End Of Word IO state
IOS0	IO State 0
PTF	Printer Flag
EBT	HPP: Eight-Bit Transfer \ = Q00000
ITS	HPP: Input to SBUS \ = LIX+MIX
nTTXENB	HPP: T-bus to A/B \ = n(LIX+MIX)
KSCANCLK	Scan clock
KSCANDET	Pressed key detected
KCn	Keyboard Columns
KRn	Keyboard Rows
nKSTOP	STOP key pressed
KLS	Keyboard interrupt ack (HP: KB Lights Strobe)
KDBENB	Keyboard Data Bus Enable

Keyboard**Display**

DEN	Display Enable
DOFF	Display Off
DCA0..2	Display Column Address
DRELA..G	Display Row Enables Left group
DRERA..G	Display Row Enables Right group
DBANK	Display Bank select
DC[0..7][a..e]	Display Column drives

Tape Drive

WCL	Write CLock
WMK	Write Mark
WDT	Write DaTa
WDA	Write Data channel A
WDB	Write Data channel B
RCL	Read CLock
RMK	Read MarK
RDT	Read DaTa
ARA	Analog Read channel A
ARB	Analog Read channel B
CIN	Cassette IN
WPT	Write PerMIT
BFD	Blank Feeder Detect
LDR	LeaDeR
CNT	CoNtrol Tape
FTC / FAST	FasT Cassette
RVC / REV	ReVerse Cassette
RNC / RUN	RuN Cassette
STOP	STOP command
LOAD	LOAD register from IO bus
WTC	Write To Cassette
CTM	ConTrol Mode
nPOPC	Power On Pulse Cassette

CTM	Control mode
MFW	Motor Forward
MRV	Motor Reverse
SFW	Solenoid Forward
SRV	Solenoid Reverse
REN	Read Enable
WEN	Write Enable
FLG	FLaG
INT	INTerrupt
DCL	Data CLock

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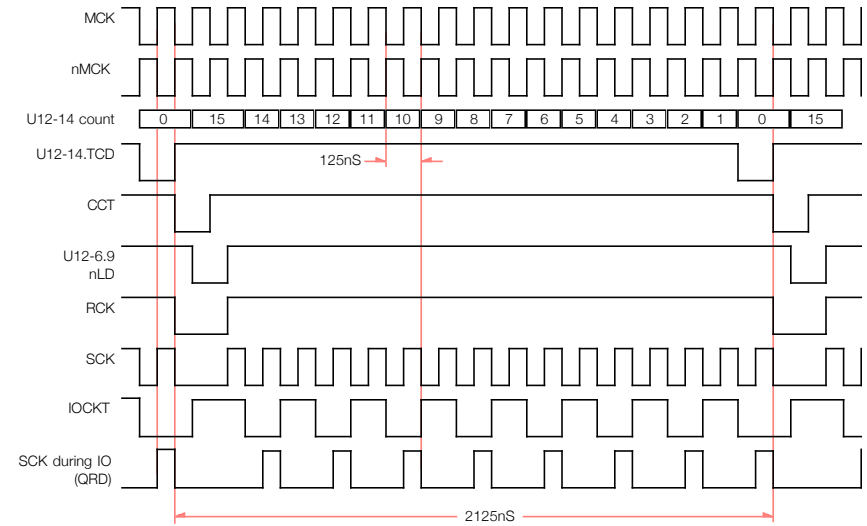
Section: Signal Names

Page: A3 Rendition: 2014 May 8

Memory Bank Address Map

Address			Binary			Maps to	Bank	Physical Location
Decimal	Octal							
0	00000	000 000	0aa	aaa	aaa		ROMB00	BASIC ROM
256	00400	000 000	1aa	aaa	aaa		ROMB00	"
512	01000	000 001	0aa	aaa	aaa		ROMB01	"
768	01400	000 001	1aa	aaa	aaa	40000	RAMB0	"
1024	02000	000 010	aaa	aaa	aaa		ROMB02	"
1536	03000						ROMB03	"
2048	04000						ROMB04	"
2560	05000						ROMB05	"
3072	06000						ROMB06	"
3584	07000						ROMB07	"
4096	10000						ROMB10	"
4608	11000						ROMB11	"
5120	12000						ROMB12	"
5632	13000						ROMB13	"
6144	14000						ROMB14	"
6656	15000						ROMB15	"
7168	16000	001 110	aaa	aaa	aaa		ROMB16	Card 26a
7680	17000	001 111	aaa	aaa	aaa		ROMB17	"
8192	20000	010 000	aaa	aaa	aaa		ROMB20	Cartridge c
8704	21000						ROMB21	"
9216	22000						ROMB22	Cartridge b
9728	23000						ROMB23	"
10240	24000						ROMB24	Card 26b
10752	25000						ROMB25	"
11264	26000						ROMB26	Cartridge a
11776	27000						ROMB27	"
12288	30000						ROMB30	Card 26c
12800	31000						ROMB31	"
13312	32000						ROMB32	Card 26d
13824	33000						ROMB33	"
14336	34000						ROMB34	Cartridge d
14848	35000						ROMB35	"
15360	36000						ROMB36	Cartridge e
15872	37000	011 111	aaa	aaa	aaa		ROMB37	"
16384	40000	100 000	0aa	aaa	aaa	01400	ROMB01	ROM Board
16640	40400	100 000	1aa	aaa	aaa		RAMB0	RAM Board rear
17408	42000	100 01a	aaa	aaa	aaa		RAMB1	"
18432	44000	100 10a	aaa	aaa	aaa		RAMB2	"
19456	46000	100 11a	aaa	aaa	aaa		RAMB3	"
20480	50000	101 00a	aaa	aaa	aaa		RAMB4	RAM Board front
21504	52000	101 01a	aaa	aaa	aaa		RAMB5	"
22528	54000	101 10a	aaa	aaa	aaa		RAMB6	"
23552	56000	101 11a	aaa	aaa	aaa		RAMB7	"
24576	60000	11a	aaa	aaa	aaa		-	unused
32767	77777	111 111 111 111 111					-	max address
		0bb	bbb	aaa	aaa	aaa		ROM
		10b	bba	aaa	aaa	aaa		RAM
		ppp	ppa	aaa	aaa	aaa		page selection

Basic Timing

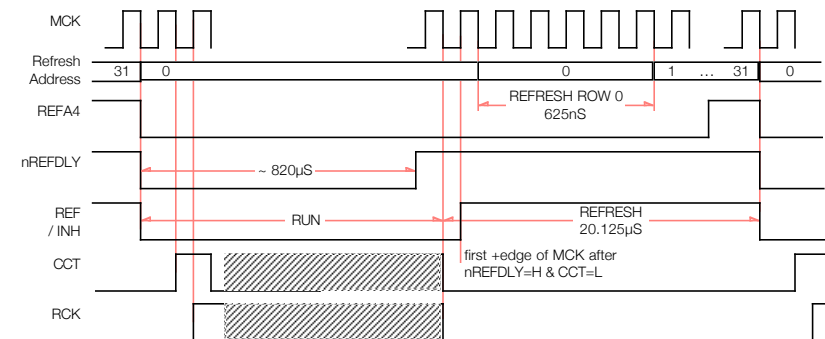


Shown is a full 16-bit microcode cycle, as defined by RCK (ROM clock). The number of pulses of SCK (bit-shift clock) within an RCK cycle, and hence the high period of RCK, is variable from 1 to 16, as determined by the binary code presented by microcode bits CC0,1,2,3.

This is an idealised presentation of the timing relationships, the real-world edge relationships will differ somewhat.

Measured values:
MCK high=60 ns, low=65nS
RCK low=180nS, lagging MCK -edge by 40nS

RAM Refresh Timing



In each refresh cycle, 32 memory access cycles are performed, one for each row in the 1103s. The refresh memory access cycles each require 5 MCK cycles. An additional MCK cycle is needed to transition into the refresh period, thus:
refresh period = (1 + 32*5) * 125nS = 20.125µS.

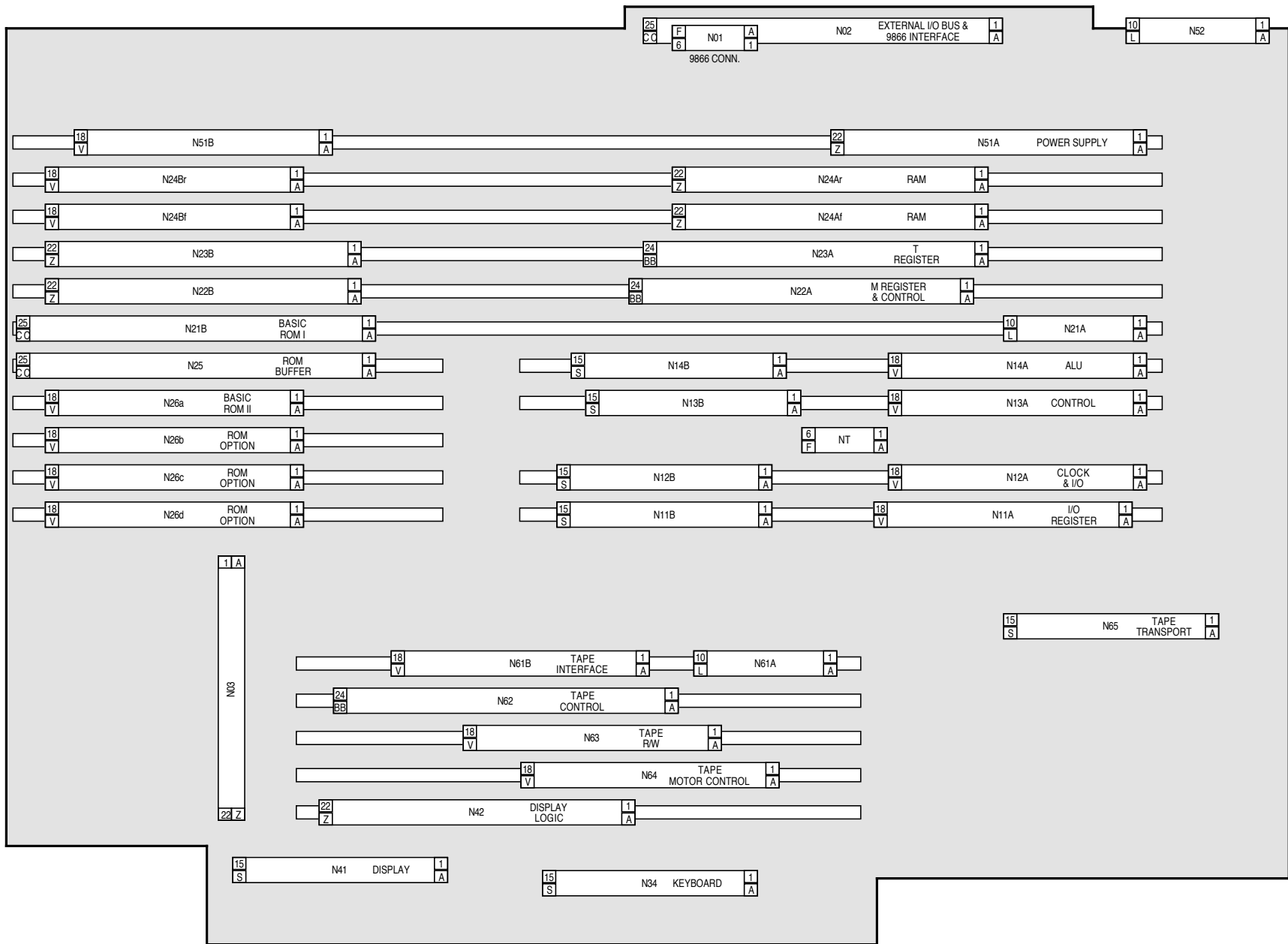
The run period is determined by the refresh delay monostable, so varies with RC tolerances. The calculated design target for the monostable is 820µS. This will be rounded out to allow completion of an RCK cycle. Each refresh cycle only refreshes half the RAM memory banks however, with a given bank being refreshed on alternate cycles. The effective refresh rate is approximately:

refresh rate = 2 * (820 + 20) = 1680µS, or 595 Hz.

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Section: Memory Map, Timing Diagrams

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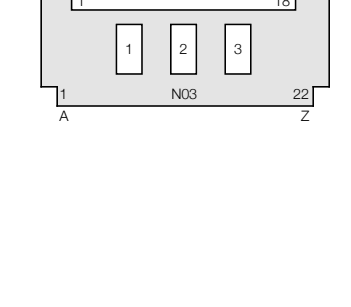
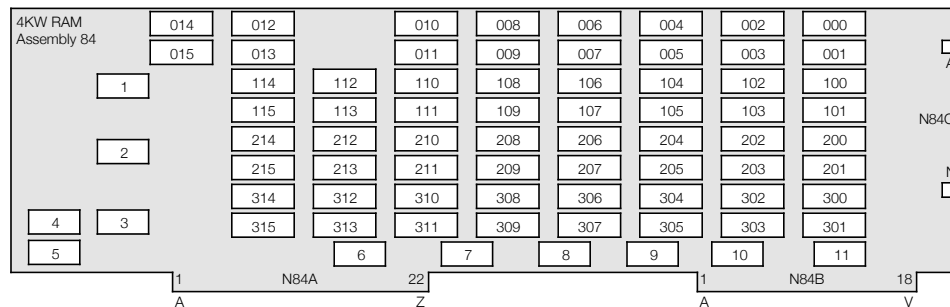
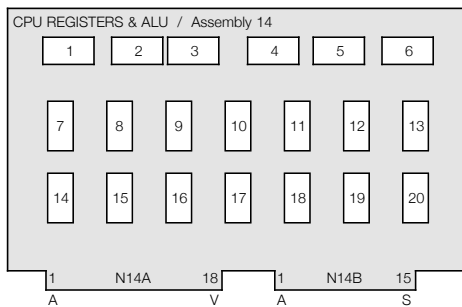
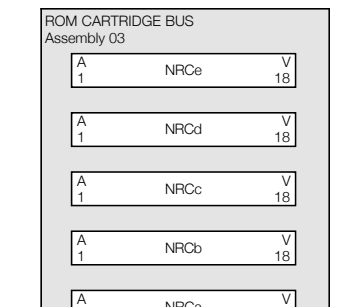
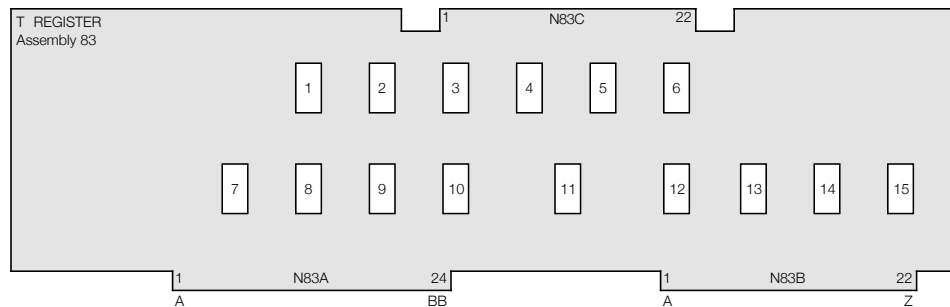
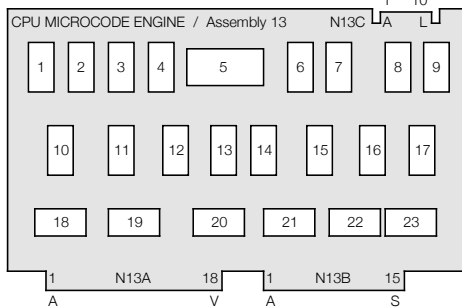
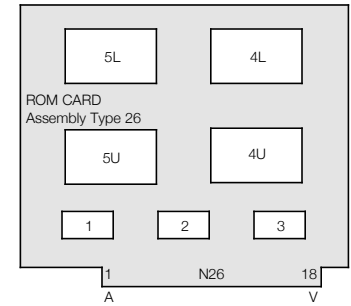
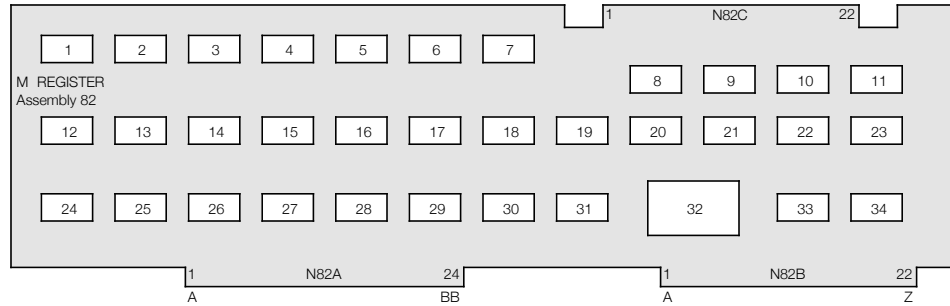
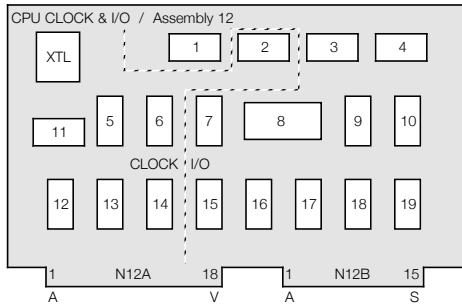
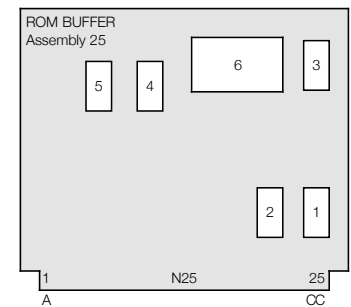
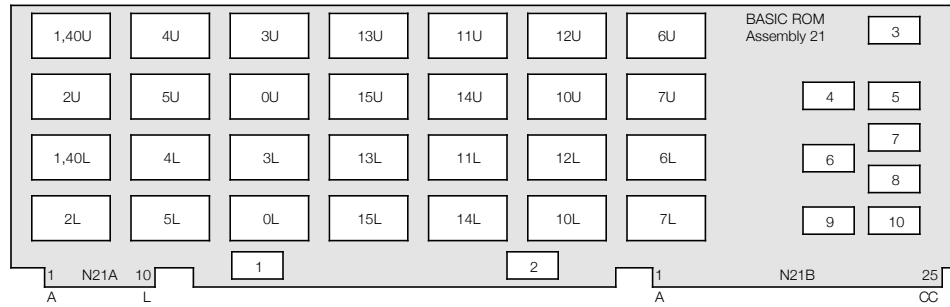
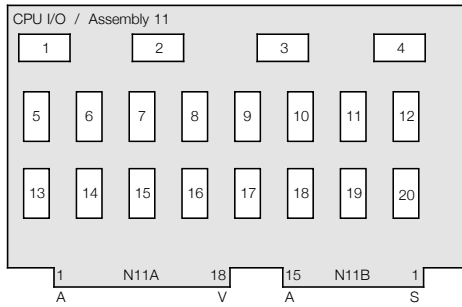
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Section: Board Layout - Backplane

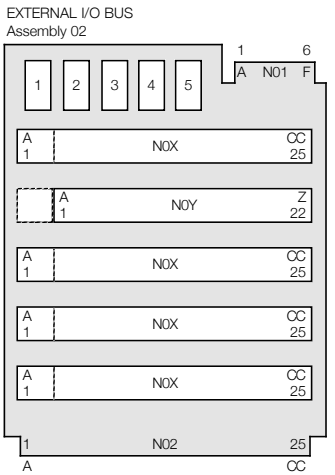
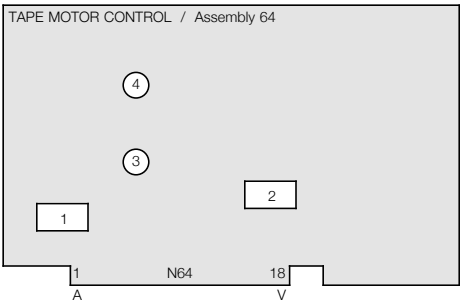
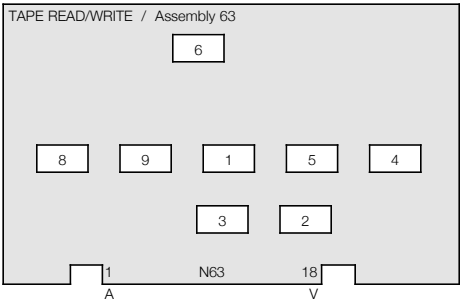
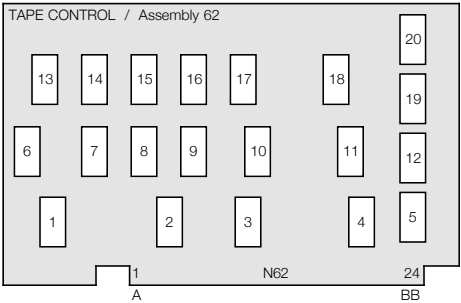
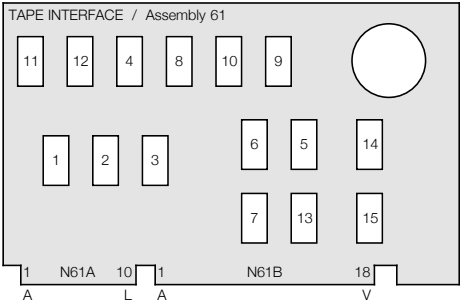
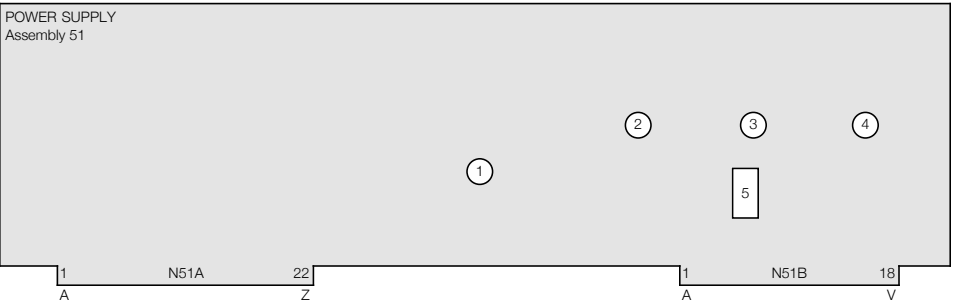
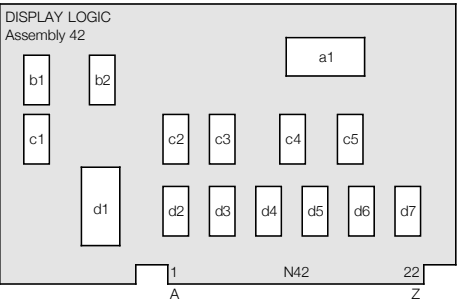
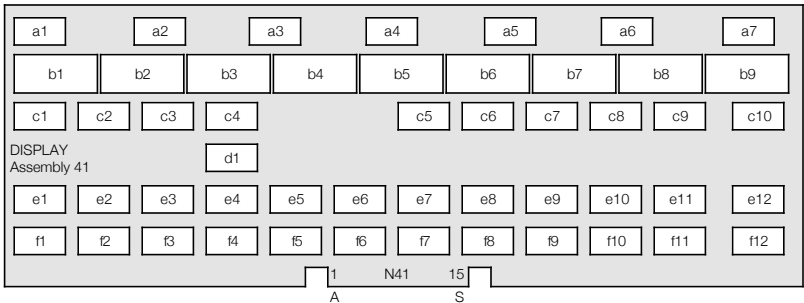
Page: L1

Rendition: 2014 May 8

BACKPLANE
TOP VIEW



• All boards as viewed from component side.



CPU ALU & REGISTERS N14A

GND	1	A	<
V+5	2	B	<
nTQR	3	C	nTTX
nTTP	4	D	AB
(TO)	5	E	TO
n(Lix+Mix)	6	F	nTRE
nTXXT	7	H	nPTR
nUTR	8	J	nTBE
SCK	9	K	nAB
nTTXENB	10	L	nXTR
-	11	M	nQTR
-	12	N	-
RCK	13	P	- (RCK)
TBUS	14	R	- (TBUS)
(MCK)	15	S	nBCD
(nCCT)	16	T	MCDIS
-	17	U	P0
-	18	V	-

N14B			
T1	1	A	AC0
-	2	B	AC2
-	3	C	Q0
-	4	D	-
T2	5	E	-
-	6	F	MCDIS
SBUS	7	H	- (<)
DC	8	J	AC1
-	9	K	-
-	10	L	T3
QAB	11	M	BC
(nPOP)	12	N	SCB
-	13	P	-
GND	14	R	<
GND	15	S	<

CPU MICROSEQ. N13A

GND	1	A	<
V+5	2	B	<
nTTX	3	C	nTQR
AB	4	D	nTTP
nUTR	5	E	nPTR
nTRE	6	F	- (MCK)
nWTM	7	H	nRDM
nTBE	8	J	- (nINH)
nAB	9	K	SCK
(-) BRC	10	L	nXTR
nQTR	11	M	- (nIPS)
(XTC)	12	N	MCDIS
RCK	13	P	Q9
Q10	14	R	TBUS
nBCD	15	S	nCCO
Q8	16	T	PO
Q4	17	U	Q5
Q6	18	V	Q7

N13B			
AC0	1	A	Q2
AC2	2	B	IQN (-)
(nHC)	3	C	Q0
Q3	4	D	Q1
QRDb	5	E	QNR
CC4	6	F	CC8
CC1	7	H	CC2
AC1	8	J	DC
nTTT	9	K	nTTM
SC1	10	L	SC0
BC	11	M	QAB
RCK	12	N	<
nPOP	13	P	nPOP
GND	14	R	<
GND	15	S	<

CPU TEST N13C

PA0	1	A	U13-5.10
PA3	2	B	PA2
PM1	3	C	PA1
SM1	4	D	PM0
SA1	5	E	SA2
-	6	F	SM2
-	7	H	PM2
-	8	J	PM3
SA0	9	K	SA3
SM0	10	L	SM3

CPU CLOCK & I/O N12A

GND	1	A	<
V+5	2	B	<
TTO	3	C	nSRA
STF	4	D	nINH
n(Lix+Mix)	5	E	- (<)
-	6	F	MCK
nPTR	7	H	- (<)
nCCT	8	J	XTC
(SCK)	9	K	SCK
nXTR	10	L	- (<)
nCEM	11	M	nIPS
RCK	12	N	<
(>)	13	P	Q9
-	14	R	-
nCCO	15	S	Q10
(>)	16	T	Q8
(>)	17	U	Q5
Q6	18	V	Q7

N12B			
(nPTF)	1	A	<
(Q4)	2	B	<
nHC	3	C	<
(>)	4	D	QRDb
CC8	5	E	<
CC4	6	F	<
CC1	7	H	CC2
(-) nCLC	8	J	IOC3
Lix+Mix	9	K	EOW
Q00000	10	L	QFG
SCB	11	M	DRC
RCK	12	N	<
CLF	13	P	nPOP
GND	14	R	<
GND	15	S	<

BACKPLANE NT

TBUS	1	A	nTTXENB
-	2	B	nCEM
nPOP	3	C	nTTXT
V+5	4	D	<
GND	5	E	<
MCDIS	6	F	Q4

CPU I/O N11A

GND	1	A	<
V+5	2	B	<
nSRA	3	C	STF
TTO	4	D	nSIH
TBUS	5	E	nCEOb
nKSTOP	6	F	nSSI
nCFI	7	H	DO15
(-) a1.8	8	J	DO14
-	9	K	DO13
(nPTF)	10	L	DO12
nDI11	11	M	DO11
nDI10	12	N	DO10
nDI9	13	P	DO9
nDI8	14	R	DO8
nDI7	15	S	DO7
nDI6	16	T	DO6
nDI5	17	U	DO5
nDI4	18	V	DO4

N11B			
nDI3	1	A	DO3
nDI2	2	B	DO2
nDI1	3	C	DO1
nDI0	4	D	DO0
Q4	5	E	Q2
Q0	6	F	nPTF
Q1	7	H	Q3
IOC3	8	J	KLS
EOW	9	K	BEEP
QFG	10	L	Q00000
DRC	11	M	QNR
nDO0	12	N	a4.6 (-)
CLF	13	P	nDEN
nPOP	14	R	a4.9 (-)
GND	15	S	<

ROM BUFFER N25

GND	1	A	<
V+5	2	B	<
V+12	3	C	ROMB20
ROMB21	4	D	ROMB22
ROMB23	5	E	ROMB24
nM13	6	F	ROMB30
M9	7	H	ROMB25
M10	8	J	ROMB26
M11	9	K	ROMB27
M12	10	L	ROMB31
nAROM	11	M	ROMB32
(V+16)	12	N	ROMB33
ROMnA8	13	P	nROMnA8b
ROMA8	14	R	nROMA8b
nROMA7	15	S	nROMA7b
nROMA6	16	T	nROMA6b
nROMA5	17	U	nROMA5b
nROMA4	18	V	nROMA4b
nROMA3	19	W	nROMA3b
nROMA2	20	X	nROMA2b
nROMA1	21	Y	nROMA1b
nROMA0	22	Z	nROMA0b
ROMB37	23	AA	ROMB35
ROMB36	24	BB	ROMB34
GND	25	CC	<

ROM CARTRIDGE BUS N03

nROMnA8b	1	A	nROMA0b
nMR7	2	B	nROMA7b
nMR5	3	C	nMAC
nMR3	4	D	nROMA2b
nMR10	5	E	nROMA4b
nMR8	6	F	-
nMR1	7	H	-
nMR12	8	J	-
nMR6	9	K	nROMA6b
nMR14	10	L	V-12
nMR4	11	M	V+5
nMR2	12	N	GND
nMR0	13	P	GND
nMR9	14	R	nROMA5b
nMR11	15	S	nROMA3b
nMR13	16	T	nROMA1b
nMR15	17	U	ROMB27
nROMA8b	18	V	ROMB22
ROMB35	19	W	ROMB23
ROMB37	20	X	ROMB20
ROMB34	21	Y	ROMB21
ROMB36	22	Z	ROMB26

ROM CARDS N26

V+5	1	A	<
V-12	2	B	nMR15
nMAC	3	C	nMR14
ROMB<lo>	4	D	nMR13
ROMB<hi>	5	E	nMR12
-	6	F	nMR11
-	7	H	nMR10
nROMnA8b	8	J	nMR9
nROMA8b	9	K	nMR8
nROMA7b	10	L	nMR7
nROMA6b	11	M	nMR6
nROMA5b	12	N	nMR5
nROMA4b	13	P	nMR4
nROMA3b	14	R	nMR3
nROMA2b	15	S	nMR2
nROMA1b	16	T	nMR1
nROMA0b	17	U	nMR0
GND	18	V	<

ROM CARTRIDGES NRC

nROMA0b	1	A	nROMnA8b
nMAC	2	B	nROMA7b
nMRC7	3	C	nROMA2b
nMRC3	4	D	nMRC5
nMRC1	5	E	nROMA4b
nMRC6	8	J	nMRC12
nMRC10	6	F	nMRC8
-	7	H	nROMA6b
nMRC6	8	J	nMRC12
V-12	9	K	nMRC14
nMRC2	10	L	nMRC4
nMRC9	11	M	nMRC0
GND	12	N	<
nROMA5b	13	P	nROMA3b
V+5	14	R	<
nMRC11	15	S	nROMA1b
nROMA8b	16	T	nMRC13
ROMB<hi>	17	U	nMRC15
ROMB<lo>	18	V	-

- : dash indicates no connection
 () : parentheses indicate backplane connection when different from board connection

TRANSFORMER N52		
a VAC	1	A
a VAC	2	B
b VAC	3	C
b VAC	4	D
c VAC	5	E
-	6	F
d VAC	7	H
-	8	J
GND	9	K
GND	10	L

POWER N51A		
a VAC	1	A
a VAC	2	B
b VAC	3	C
b VAC	4	D
c VAC	5	E
d VAC	6	F
GND	7	H
GND	8	J
GND	9	K
GND	10	L
GND	11	M
GND	12	N
V+5SENSE	13	P
V+5	14	R
V+5	15	S
V+5	16	T
V+UH	17	U
V+12S	18	V
V+17	19	W
MGND	20	X
MDB	21	Y
MDE	22	Z

N51B		
GND	1	A
GND	2	B
V+12	3	C
V+12SENSE	4	D
- *	5	E
GNDSENSE	6	F
-	7	H
nPOP	8	J
V+16SENSE	9	K
GNDSENSE	10	L
V+16	11	M
V+19.5	12	N
GNDSENSE	13	P
V-12SENSE	14	R
V-12	15	S
GND	16	T
GND	17	U
GND	18	V

RAM N24A		
GND	1	A
V+5	2	B
(V+UH)	3	C
V-12	4	D
RAMB3/7	5	E
RAMB2/6	6	F
RAMB1/5	7	H
RAMB0/4	8	J
(>)	9	K
(>)	10	L
GND	11	M
GND	12	N
V+5SENSE	13	P
V+5	14	R
V+5	15	S
V+5	16	T
V+UH	17	U
V+12S	18	V
V+17	19	W
MCA	20	X
MAC	21	Y
GND	22	Z

N24B		
GND	1	A
RAMRf/r	2	B
-	3	C
(GND)	4	D
-	5	E
V+16	6	F
V+16	7	H
V+19.5	8	J
(N23B.13)	9	K
nMW7	10	L
nMW6	11	M
nMW5	12	N
nMW4	13	P
nMW3	14	R
nMW2	15	S
nMW1	16	T
nMW0	17	U
GND	18	V

RAM 4K TEST N24C		
RAMA3/A1	1	A
RAMA4/A2	2	B
B0.nPC	3	C
nRAMA5/A7	4	D
nRAMA8/A5	5	E
nRAMA6/A8	6	F
B1.RnW	7	H
B2.nPC	8	J
nRAMA7/A9	9	K
B3.nPC	10	L
B3.RnW	11	M
B3.nCE	12	N

T REGISTER N23A		
GND	1	A
V+5	2	B
(V+UH)	3	C
-	4	D
-	5	E
>	6	F
nWTM	7	H
SCK	8	J
(nRAMA0)	9	K
(nRAMA3)	10	L
nMW15	11	M
nMW14	12	N
nMW13	13	P
nMW12	14	R
nMW11	15	S
nMW10	16	T
nMW9	17	U
nMW8	18	V
(>)	19	W
-	20	X
SCO	21	Y
nEDT	22	Z
XIN	23	AA
GND	24	BB

N23B		
GND	1	A
(V+12)	2	B
(V-12)	3	C
TPC	4	D
-	5	E
-	6	F
-	7	H
-	8	J
-	9	K
-	10	L
(V+16)	11	M
-	12	N
(N24B.9)	13	P
nMW7	14	R
nMW6	15	S
nMW5	16	T
nMW4	17	U
nMW3	18	V
nMW2	19	W
nMW1	20	X
nMW0	21	Y
GND	22	Z

M REGISTER N22A		
GND	1	A
V+5	2	B
nROMB00	3	C
nROMB03	4	D
nROMB05	5	E
nWTM	6	F
SCK	7	H
nRAMA0	8	J
nRAMA3	9	K
nRAMA4	10	L
nRAMA1	11	M
nRAMA2	12	N
RAMA8	13	P
RAMA9	14	R
RAMA5	15	S
RAMA6	16	T
RAMA7	17	U
RWT	18	V
MCA	19	W
MAC	20	X
MSTL	21	Y
(-) 3.1	22	Z
M0	23	AA
GND	24	BB

N22B		
GND	1	A
V+12	2	B
TPC	3	C
(N23B.D)	4	D
-	5	E
-	6	F
nREFDLY	7	H
nREFDLY	8	J
RAMRf	9	K
RAMRf	10	L
V+16	11	M
ROMB16	12	N
ROMB17	13	P
nROMB06	14	R
nROMB07	15	S
nROMB10	16	T
nROMB11	17	U
nROMB12	18	V
nROMB15	19	W
nROMB14	20	X
nROMB13	21	Y
GND	22	Z

BASIC ROM I N21A		
GND	1	A
GND	2	B
V+5	3	C
V+5	4	D
nROMB05	5	E
nROMB03	6	F
nROMB00	7	H
nROMB01	8	J
nROMB02	9	K
nROMB04	10	L

N21B		
>	1	A
>	2	B
>	3	C
>	4	D
>	5	E
>	6	F
>	7	H
>	8	J
nROMB6	9	K
nROMB7	10	L
>	11	M
RE3	12	N
ROMA8	13	P
nROMA7	14	R
nROMA6	15	S
nROMA5	16	T
nROMA4	17	U
nROMA3	18	V
nROMA2	19	W
nROMA1	20	X
nROMA0	21	Y
nROMB11	22	Z
nROMB15	23	AA
nROMB13	24	BB
>	25	CC

M REG TEST N22C		
AEN	1	A
MONO.C	2	B
UB2-4.6	3	C
MONO.RC	4	D
-	5	E
-	6	F
M15	7	H
M14	8	J
M13	9	K
M12	10	L
M11	11	M
M10	12	N
M9	13	P
M8	14	R
M7	15	S
M6	16	T
M5	17	U
M4	18	V
M3	19	W
M2	20	X
M1	21	Y
M0	22	Z

T REG TEST N23C		
T15	1	A
T11	2	B
-	3	C
T10	4	D
T14	5	E
T13	6	F
T9	7	H
T8	8	J
T12	9	K
T7	10	L
-	11	M
-	12	N
T6	13	P
T4	14	R
T5	15	S
-	16	T
T0	17	U
T1	18	V
T3	19	W
-	20	X
-	21	Y
T2	22	Z

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